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HIGH SPEED DATA ACQUISITION SYSTEM: BURST-TYPE PHENOMENA WITH WAIT PERIODS IN BETWEEN

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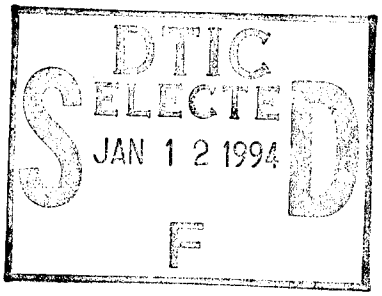

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In some aerospace applications data periodically occurs in short bursts. High frequency content data can be digitized and prepared for transmission at a much lower bit rate during the intervals between bursts. The analog burst signal is digitized by a high-speed analog-to-digital converter to produce binary words which are stored in a FIFO memory along with synchronization words which mark the beginning of every new frame. The stored words are then converted into a serial bit stream during the wait periods and put into a PCM format for transmission to the ground. In this thesis, the system is tested with a data collection period of 16.0 μsec and a wait period of 5.136 msec. A commercial converter is used to sample at 20 MHz and produce 10-bit words which are read out at a 62.5 kilo word per second rate. Experimentally, it was found that the system developed provided accuracy with 1.2% error for signal with fast rise and fall times, signals with slow rise and fall times, $e^{-t/\tau}$ wave-functions, and pseudo-random signals.

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1. INTRODUCTION

The high frequency content of the analog signals from scientific experiments, as well as the video cameras carried on balloons, sounding rockets, space shuttles and satellites are usually converted into digital signals. The digital signals are then transmitted back to the ground station in a pulse-code-modulation (PCM) binary bit stream format. In some space applications, however, data is taken during burst-type phenomena with wait periods in between. The period in which the data is collected is determined by the period when the scientific instruments are required to take data. The data collection periods are becoming shorter and the frequency content of the signals are becoming higher.

This thesis utilizes state-of-the-art commercial components for a possible high-speed data acquisition system. During the burst interval, a sampling analog-to-digital converter (ADC) digitizes the incoming signal to produce digital words. Preceding the data words, synchronization patterns (or SYNC words) are inserted into a First-In-First-Out (FIFO) memory to mark the beginning of the data frame. Once the SYNC words are inserted, the digital words from the ADC are then inserted into the FIFO memory for temporary storage. During the quiet periods, the high-speed burst digital words can be reformatted into a PCM binary serial bit stream and transmitted at a slower rate determined by the wait period.

The system developed here is tested with a 16.0 μsec data gathering burst interval with a wait period of 5.136 msec.

These values were chosen arbitrarily. It utilizes a commercially available analog-to-digital converter capable of sampling data sources as high as 60 mega-samples per second (MSPS) with 10-bit accuracy. Here, a 20-MSPS was chosen for testing the concept. Figure 1 shows the block diagram of the system used to provide high sampling rates for specified short periods of time and whose output provides low rate PCM signals. The "flash" ADC digitizes the

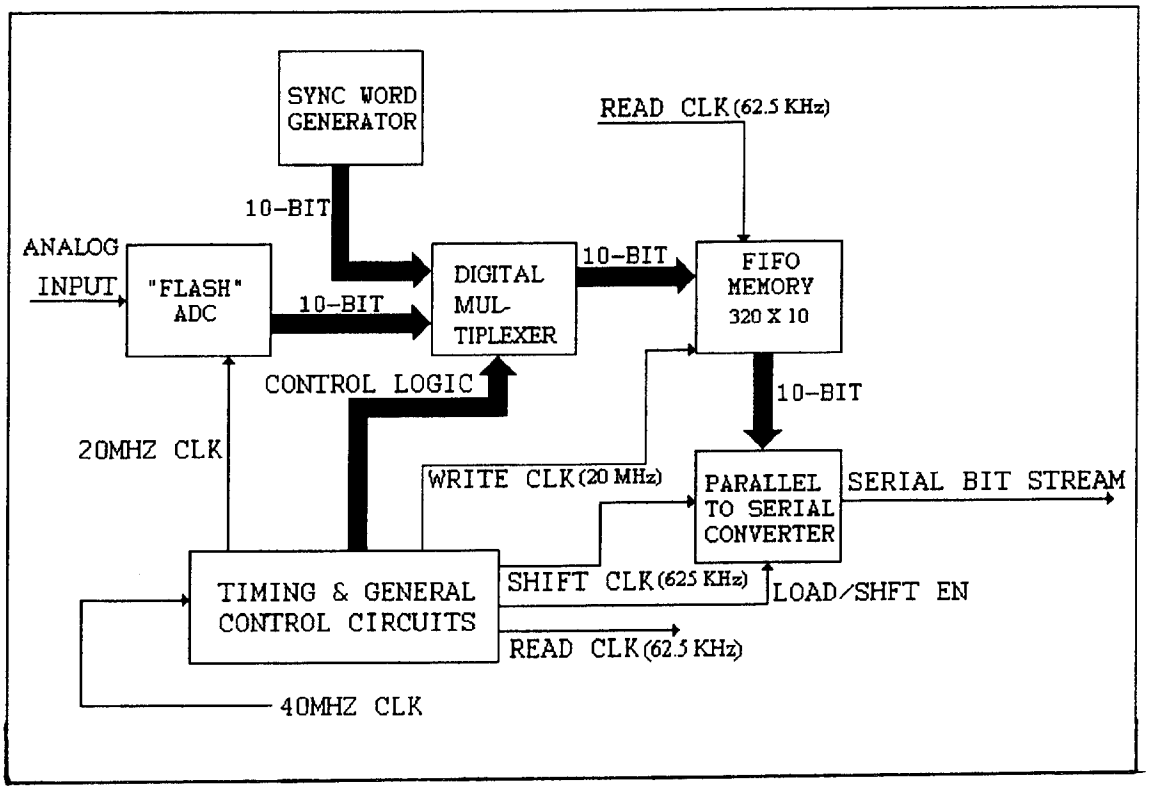


Figure 1. High-Speed Data Acquisition System

incoming signal at 20 MSPS for 16.0 μsec to produce 320 10-bit parallel words. At the beginning of each new frame, two 10-bit SYNC words from the SYNC word generator are inserted into the FIFO memory. A digital multiplexer is used to control the selection of the data words between the flash ADC and SYNC word generator. Once the two SYNC words are inserted into the FIFO memory, the data words from the flash ADC are also inserted into the FIFO memory for temporary storage. Thus, there are two SYNC words plus 318 samples being stored in the FIFO memory for each burst interval of 16.0 μsec . The high-speed data stored in the FIFO is then loaded into the parallel-to-serial converter at a rate of 62.5 KHz. The parallel-to-serial converter converts the stored parallel words into a serial bit stream and clocks the data out at a rate of 625 KHz for 5.136 msec. This results in a continuous PCM serial bit stream.

For ease in presentation, this thesis is divided into six chapters. In Chapter 2, high-speed data acquisition systems in burst-type phenomena with wait periods in between are discussed. The need of a flash ADC to generate digital data is demonstrated in Chapter 3. High-speed memory and control circuitry used are shown in Chapter 4. The analysis of the experimental results of this system, and the conclusions and recommendations reached are given in Chapters 5 and 6 respectively.

2. HIGH-SPEED DATA ACQUISITION IN BURST-TYPE PHENOMENA WITH WAIT PERIODS IN BETWEEN

In many scientific experiments conducted in space, data is collected intermittently. The period in which the data is collected may be small compared to the complete time of the flight. Continuous sampling of the signal for PCM binary bit stream in r-f transmission is not only unnecessary but wasteful. Furthermore, the frequency content of the signals to be sampled has steadily increased for the past decade. Thus, PCM bit rate in which the data is transmitted has also increased. In other words, some of the data collection periods are becoming shorter and the frequency content of the signals are becoming higher. This leads to unnecessary increase in transmission bandwidth and reduction in signal-to-noise ratio (SNR). In many aerospace telemetry systems, PCM bit rates routinely exceed 1 mega-bits per second (MBPS). Future systems are expected to require even higher rates. The need to transmit high-frequency content burst signals with a lower rate PCM binary bit stream in r-f transmission during between-burst intervals becomes mandatory when r-f transmission bandwidth must be conserved.

To demonstrate the concept of conserving the r-f transmission bandwidth, arbitrary values of a 16.0 μsec data gathering burst interval and a wait period of 5.136 msec were chosen. Figure 2 shows a timing diagram of this system. In Figure 2(a), the system samples the incoming signal to produce digital words. To

avoid aliasing, the sampling rate of the system must satisfy the Nyquist rate criterion. To simulate a high-speed data acquisition system, a 20 MHz sampling rate was chosen to be used on the system. In general, a real signal is not band limited. The sampling rate of the system must be higher than twice the highest frequency component of the signal. Thus, two times the highest frequency of the test signal must be small compared to the sampling rate of the system in order to avoid aliasing [9]. the digital word size is chosen to be 10-bits yielding an accuracy of approximately 0.1% which is more than adequate for most instrumentation. This means there are exactly 320 10-bit parallel words being produced in a burst interval of 16.0 μsec.

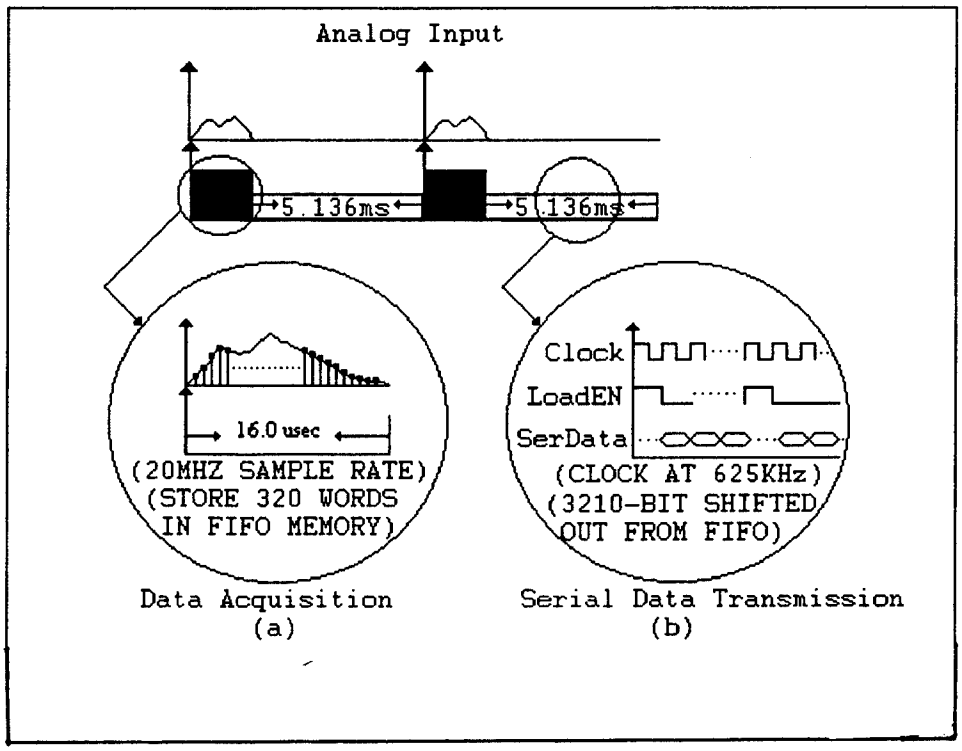


Figure 2. Burst-type Phenomena With Wait Periods in Between

In general, the synchronization pattern or SYNC word is inserted into the high-speed FIFO memory before the 10-bit parallel data words are stored. The SYNC word is used to mark the beginning of the frame, and it is repeatedly inserted for every new frame. The typical PCM format is shown in Figure 3. Data words are grouped into blocks known as frames with a unique SYNC word at the beginning of each frame. For most PCM data formats, a pattern of only one word length is sufficient due to the relatively high probability of random data matching the SYNC word. It is normally desirable to choose a frame synchronization pattern that is a multiple of the word length. Thus, this system uses two identical standard 10-bit words for the synchronization pattern. This standard 10-bit synchronization pattern is 11 0111 0000, which is adapted by the Inter-Range Instrumentation Group (IRIG) committee as an optimal pattern for a 10-bit system [8]. Figure 4 shows the PCM format of the system described in this thesis.

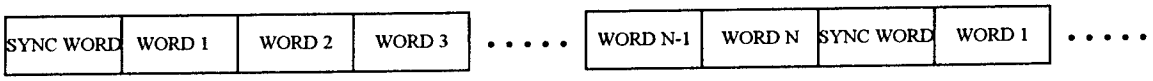


Figure 3. Typical PCM Format

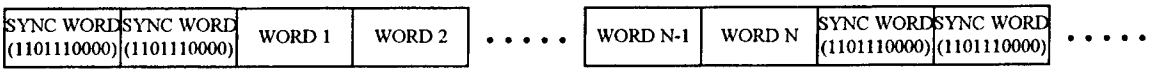


Figure 4. PCM Data Format of the System

In order to store the data correctly, the write cycle of the high-speed FIFO memory must operate at the same rate as the sampling rate of the system. This will ensure each conversion is shifted into the FIFO for temporary storage. Since the burst interval only lasts for 16.0 μsec, there are exactly two SYNC words plus 318 data words being stored in the FIFO memory. Finally, the high-speed burst data stored in the FIFO is converted to a serial bit stream and clocked out continuously. To demonstrate the concept of conserving the transmission bandwidth, a much slower PCM rate (625 KHz) compared to the sampling rate of the system was chosen. In order to completely empty out all 3200-bits from the FIFO, the minimum requirement for the quiet interval must equal to 5.12 msec. The quiet interval can be calculated as follows:

$$\text{Quiet Interval} \geq \text{Number of Bits/Clock Rate} \qquad (1)$$

A larger interval, of course, can be used to empty out all its data from the FIFO memory. Thus, 5.136 msec will serially shift out 3210-bits for this system with the last 10-bits being the filler data as shown in Figure 2(b). The filler data is actually useful for decommutation purposes. Since most modern decommutator units treat these SYNC words as one word, it is a good rule of thumb to have an even number of words. The filler data is arbitrarily chosen to be all zeros for this system.

To implement this system, a high rate sampling flash ADC and a high-speed FIFO memory are required. The next chapter discusses the AD9020/PCB evaluation board to generate digital data.

3. ANALOG-TO-DIGITAL CONVERTER (ADC)

The need for higher-speed analog-to-digital converters is growing due to the enormous increase in digital signal processing, instrumentation, control, high definition TV, and aerospace telemetry applications. Some of the major types of ADCs are flash, successive approximation, counting or tracking, single/double slope, pipeline algorithmic, and converters using sigma-delta modulation [4].

For high conversion speed and dynamic performance, a "flash" ADC is the best choice. Its applications range from ultrasound medical imaging to radar and communication receivers. A block diagram of a typical flash converter is shown in Figure 5. The flash converter consists of 2^N-1 comparators connected in parallel, where N is the number of bits. The analog input signal to be digitized is applied to all latched comparators simultaneously. The reference voltage for each comparator is derived from a resistive divider. The reference voltage for each comparator is one least significant bit (LSB) higher than the comparator immediately below it. When an analog input is present at the input of a comparator bank, the comparators with a reference voltage below the level of the input signal will assume a logic "1" output. The comparators with reference voltage above the input signal will assume a logic "0" output. The latched comparators' outputs are then combined by a priority encoder to form parallel N-bit digital words. The complete conversion requires only one clock-cycle to

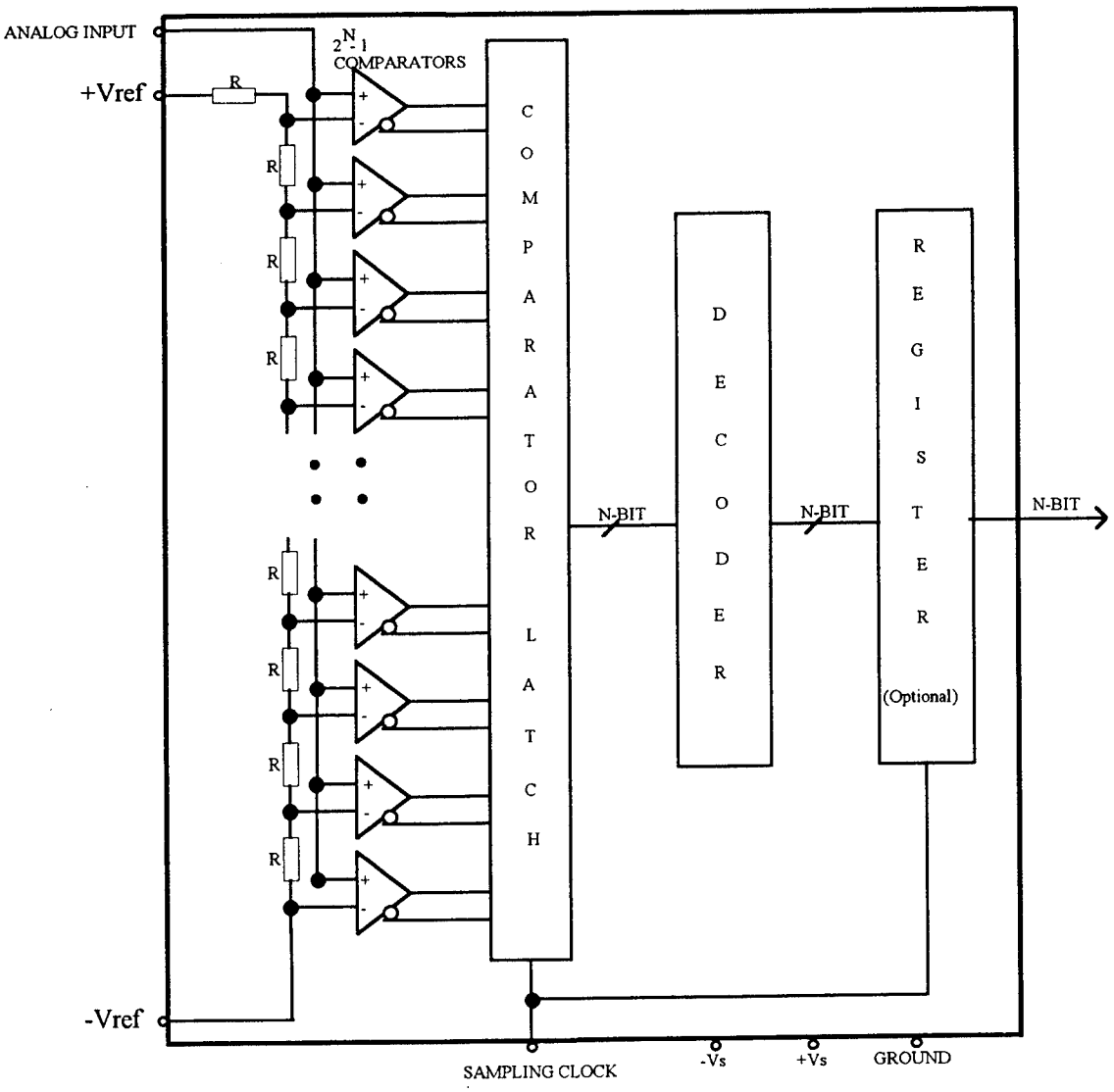


Figure 5. N-Bit Flash Converter

complete. This entire process is also known as direct conversion [1].

The space, input capacitance, and power required by a large number of comparators have historically limited the resolution available with direct conversion. For this reason, most of the converters used today are either partial direct converters or modified direct converters.

In this thesis, a modified direct converter is utilized. This converter, called the flash AD9020 converter, uses fewer comparators than the classical direct converter and requires two clock-cycles to complete an analog-to-digital conversion. The analog-to-digital conversion for the nine most significant bits is performed by 512 comparators. The value of the least significant bit is determined by a unique interpolation scheme between adjacent comparators. The proprietary information of the interpolation scheme is owned by Analog Devices. The AD9020 was chosen since it is economically affordable for this thesis, and it also provides high conversion speed and dynamic performance. A functional block diagram of an AD9020 converter is shown in Figure 6. Unlike the classical flash converters which require 2^N-1 comparators for N-bit resolution, the AD9020 requires only $(2^N-1)/2$ or 512 comparators for a 10-bit resolution [3]. By using 512 comparators, the AD9020 reduces input capacitance and improves linearity. The analog input range is determined by an external voltage reference ($+V_{ref}$ and $-V_{ref}$) normally $\pm$ 1.75V. Thus, the test signal input level used in this thesis cannot have a peak value greater than $\pm$ 1.75V. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. Taps along the resistor ladder ($1/4_{ref}$, $1/2_{ref}$ and $3/4_{ref}$) are provided to optimize linearity. Rated performance is achieved by driving the $1/4_{ref}$, $1/2_{ref}$ and $3/4_{ref}$ points at 1/4, 1/2 and 3/4 of the voltage reference range, respectively. The converter is also capable of sampling rates of

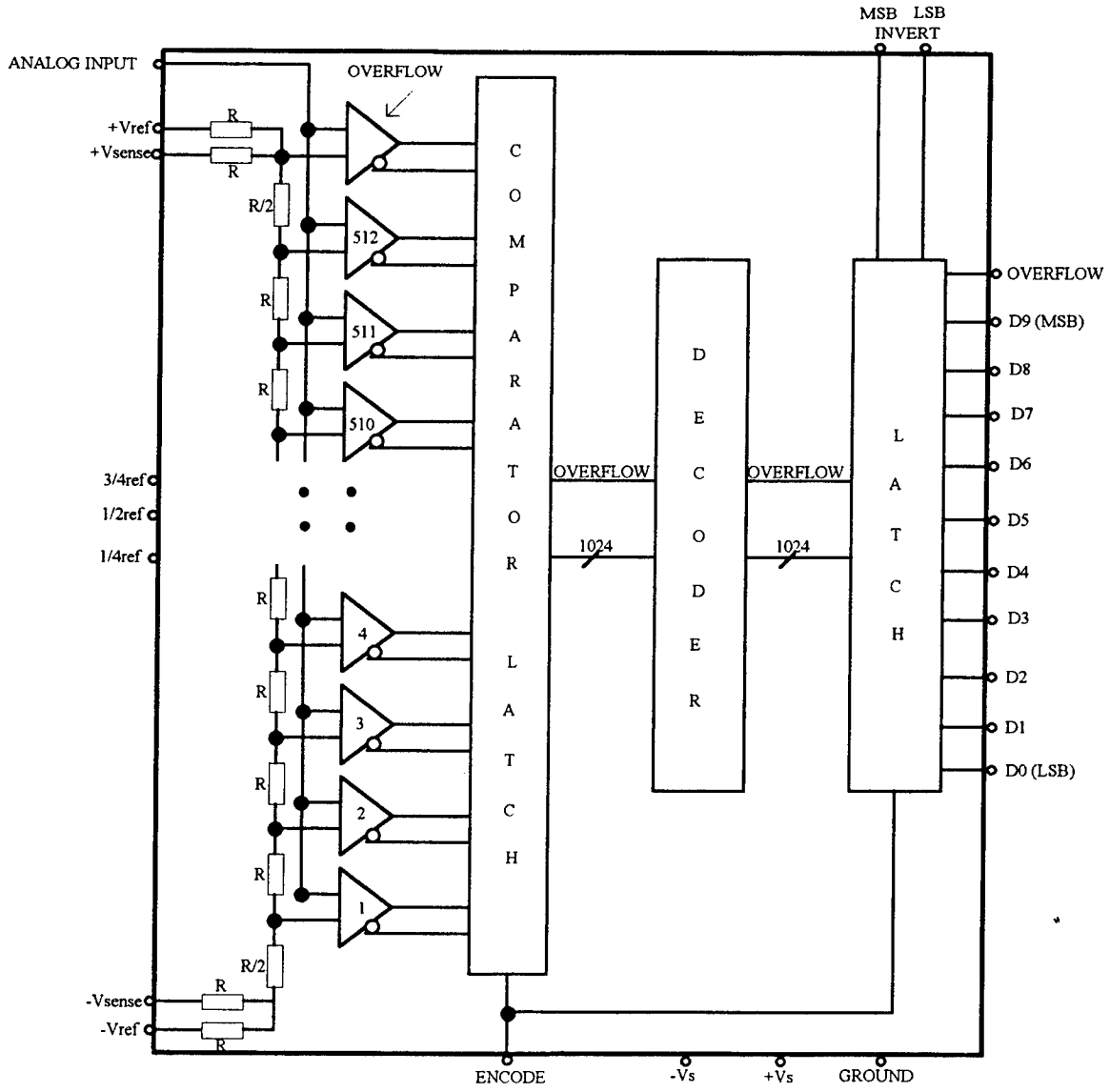


Figure 6. Functional Block Diagram of an AD9020 Converter

60 MSPS. It has a DC differential non-linearity of 0.75 LSB and a DC integral non-linearity od 1.0 LSB [1]. It is considered to be one of the best converters available for high-speed data acquisition applications in the market for a 10-bit resolution system [5].

Since most high-speed converters have an optional printed circuit board (PCB) packaged with supportive circuits, the AD9020 was purchased with this option. The AD9020/PCB evaluation board contains circuitry for buffering the input signal, generating reference voltages, registering output data and reconstructing the quantized signal with an AD9713 digital-to-analog converter (DAC). The evaluation board requires the following four individual power sources: +5V ALG, -5.2V ALG, +5V DIG and -5.2V DIG. ALG denotes the voltage source used to power the analog portions of the circuitry, whereas DIG denotes the voltage source used for the digital portion. It consumes approximately 1.145 watts of power. The 10-bit buffered data is available with strobe signal via a 37-connector [2]. Figure 7 shows a schematic diagram of this board.

The components on this board are used to sample the incoming signal at the rate of 20 MSPS and produce the 10-bit parallel words which are loaded into the high-speed FIFO memory. An evaluation of this board will be covered in Chapter 5.

The next chapter discusses the requirements for high-speed FIFO memory and control circuitry to store data from the AD9020/PCB evaluation board correctly.

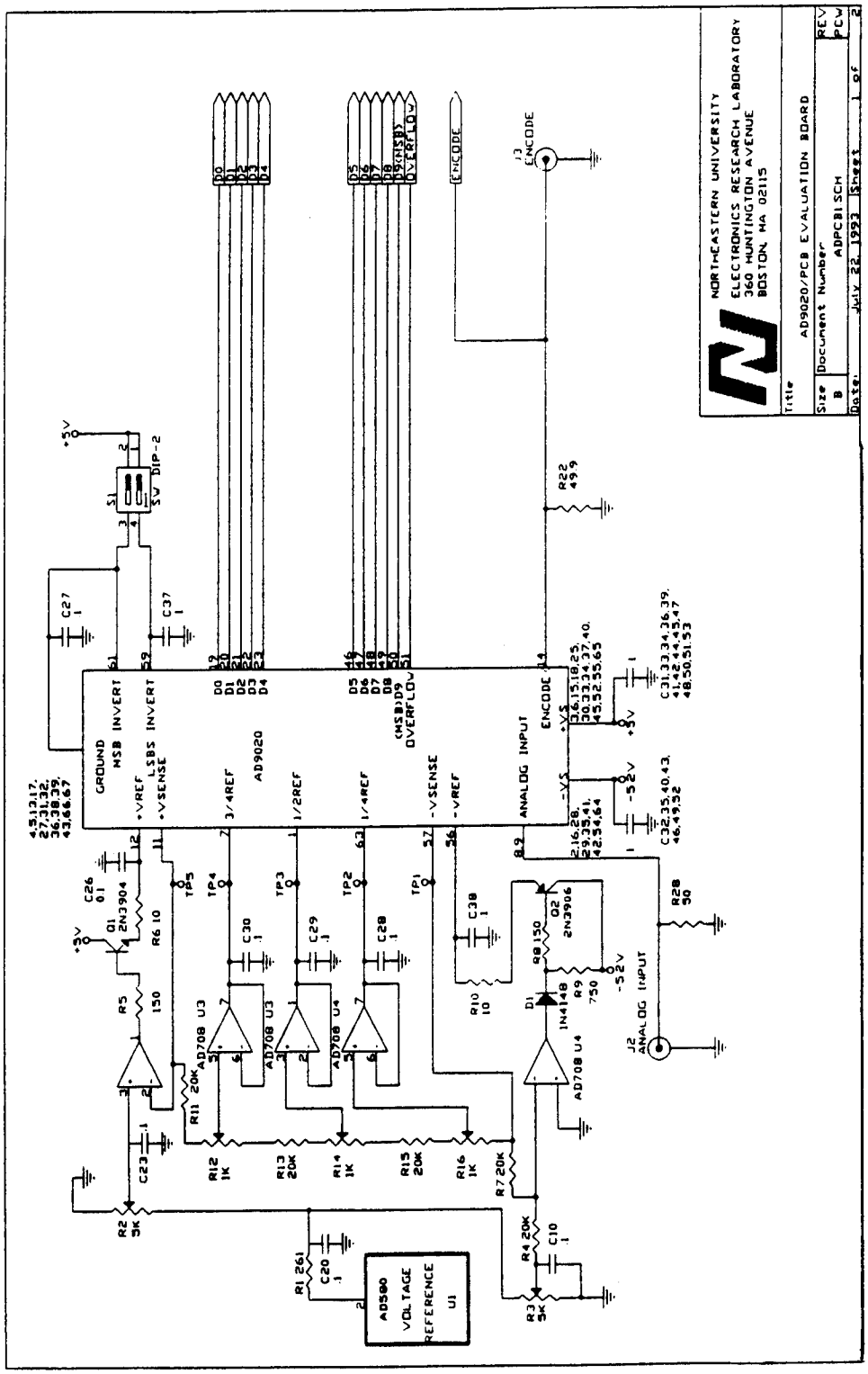


Figure 7(a). AD9020/PCB Evaluation Board Schematic Diagram

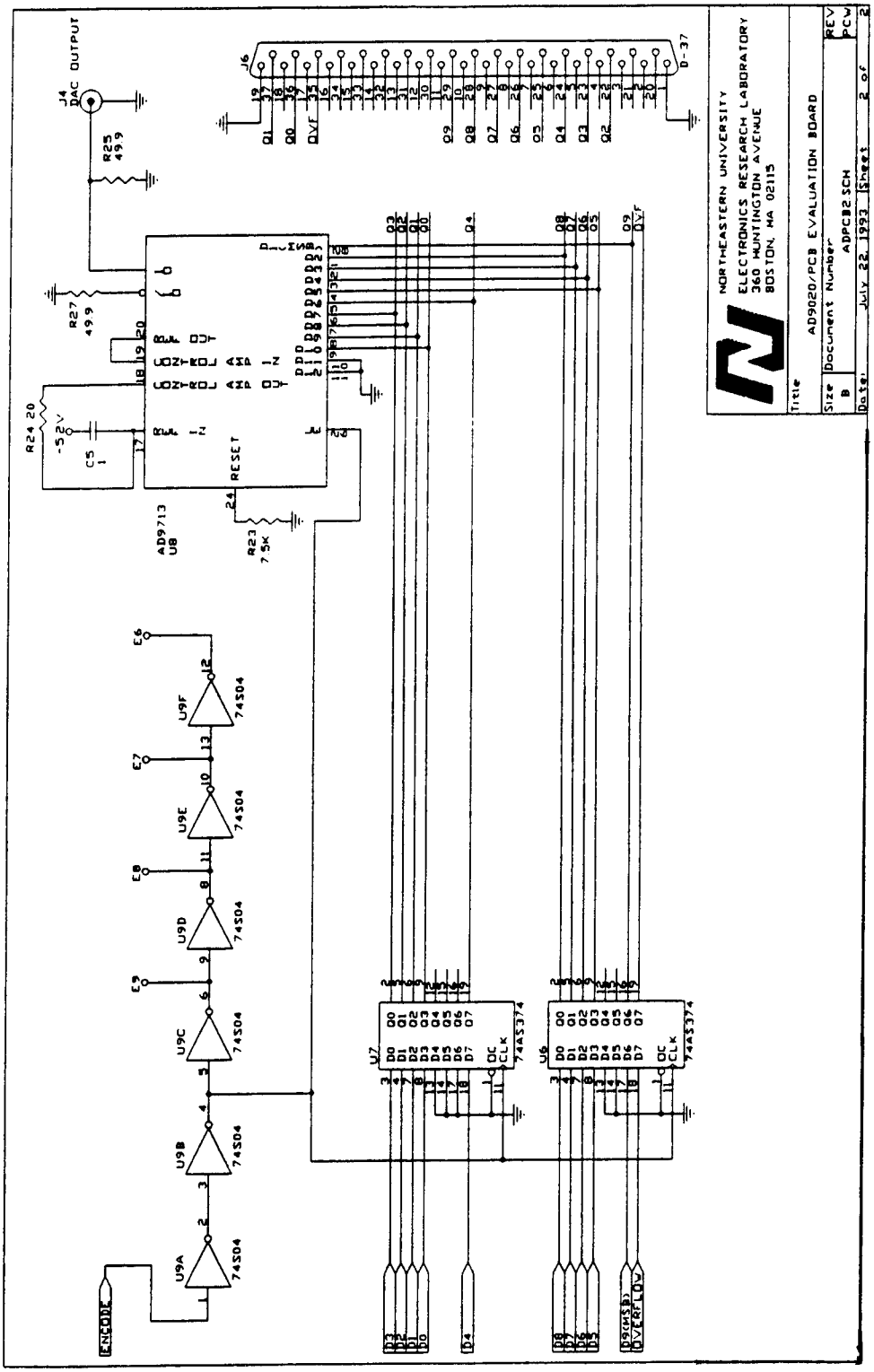


Figure 7(b). AD9020/PCB Evaluation Board Schematic Diagram

4. HIGH-SPEED FIFO MEMORY AND CONTROL CIRCUITRY

The word rate of the AD9020/PCB is 20 MSPS producing 200 MBPS of information. Thus, high-speed FIFO memory is required. The high-speed FIFO memory being used here is an IDT72104 asynchronous FIFO. It is a high-speed parallel-to-serial, serial-to-serial, serial-to-parallel, or parallel-to-parallel 4K X 9 FIFO. It has been designed to provide expansion in both depth and width. The IDT72104 can clock data in and out simultaneously at different clock rates (asynchronous clocking), and can also operate at rates as high as 50 MHz with minimum cycle time of 35 nsec [6]. It was manufactured by Integrated Device Technology. Figure 8 shows a functional block diagram of the memory.

In this system, the IDT72104 FIFO memory is used in a parallel-to-parallel configuration. Since the IDT72104 is configured as a 4K X 9 FIFO memory, the system requires two FIFOs in order to store the 10-bit parallel words from the AD9020/PCB. Thus, 4K 18-bit words could be stored if needed. The write clock for the FIFO must also be operated at the same rate as the sampling rate (20 MHz) of the ADC. This will ensure each conversion from the ADC is shifted into the FIFO for temporary storage (see Figure 9 for a complete timing diagram of the write cycle of this system). The read clock for the FIFO will be operating at a rate of 62.5 KHz. The read clock rate is 320 times slower than the write clock of the FIFO memory. The purpose of using a slower read clock is to demonstrate the idea of burst-type phenomena with very long wait periods in between, therefore, illustrating that the overall PCM bit rates can

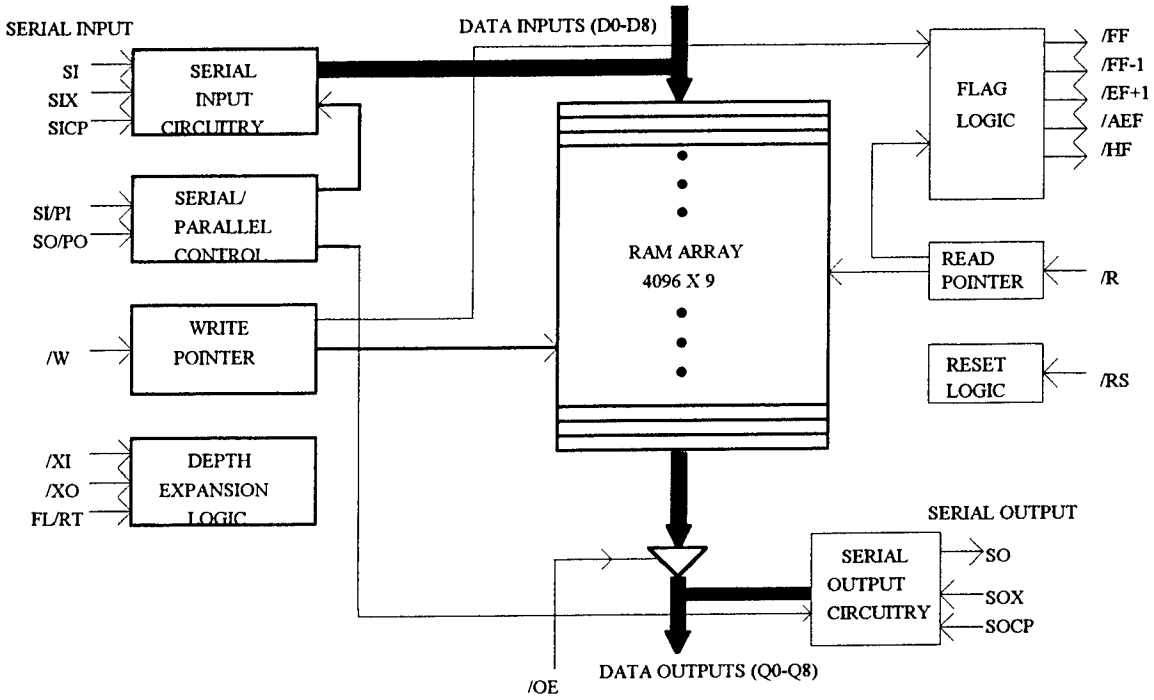


Figure 8. Functional Block Diagram of an IDT72104

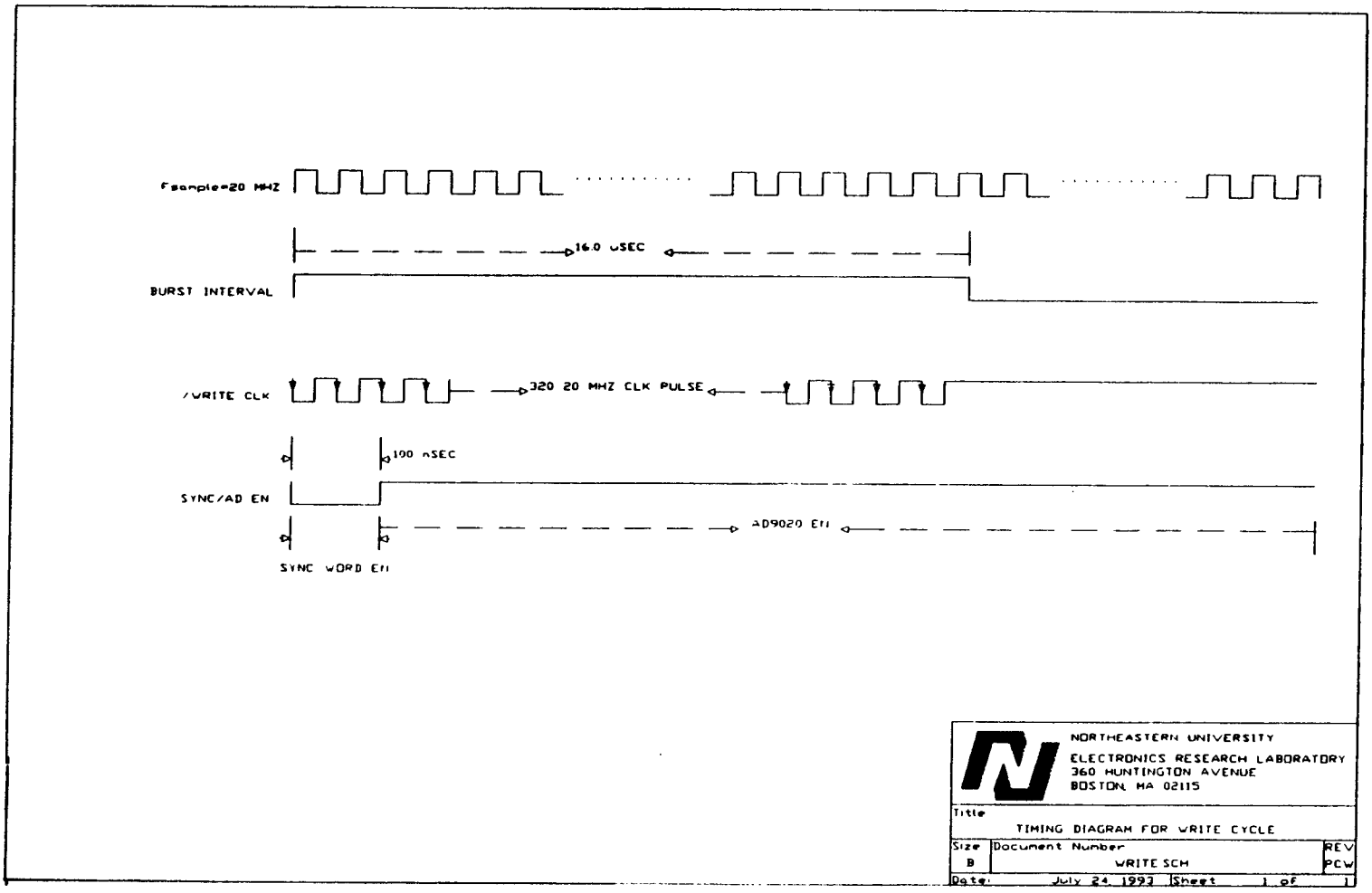


Figure 9. Timing Diagram for Storing Data Words Into FIFO Memory

be reduced for r-f transmission. Once the required data is stored in the FIFO from the SYNC word generator and the AD9020/PCB, the FIFO outputs the stored data for 5.12 msec to the parallel-to-serial converter. The parallel-to-serial converter converts the data into a serial bit stream. After the 320 words are completely converted and shifted out by the parallel-to-serial converter, the 10-bit filler data is also shifted out from the parallel-to-serial converter for 0.016 msec. The total time required to serially shift out 3210-bits from the parallel-to-serial converter is 5.136 msec. Thus, the shift clock of the parallel-to-serial converter must be 10 times the rate of the read clock (62.5 KHz) of the FIFO. This will ensure each 10-bit parallel word is converted to a 10-bit serial bit stream properly. Figure 10 shows a timing diagram of the read and shift clocks of the system.

All the timing and control signals are generated by binary counters and EPROM, respectively. Figure 11 shows the block diagram of this design. The binary counter circuitry clocked at 40 MHz generates the 20 MHz sampling rate for the AD9020/PCB. A 180° phase shift of the sampling clock is also generated for the write clock of the FIFO memory. The read clock is generated by dividing the 40 MHz input clock by 640, whereas the shift clock is the input clock divided by 64. The EPROM generates the following required control signals: Write/Read-Enable, Load/Shift-Enable, SYNC/AD-Enable. The Write/Read-Enable is used to initiate the AD9020/PCB to sample the incoming signal. A low pulse of the

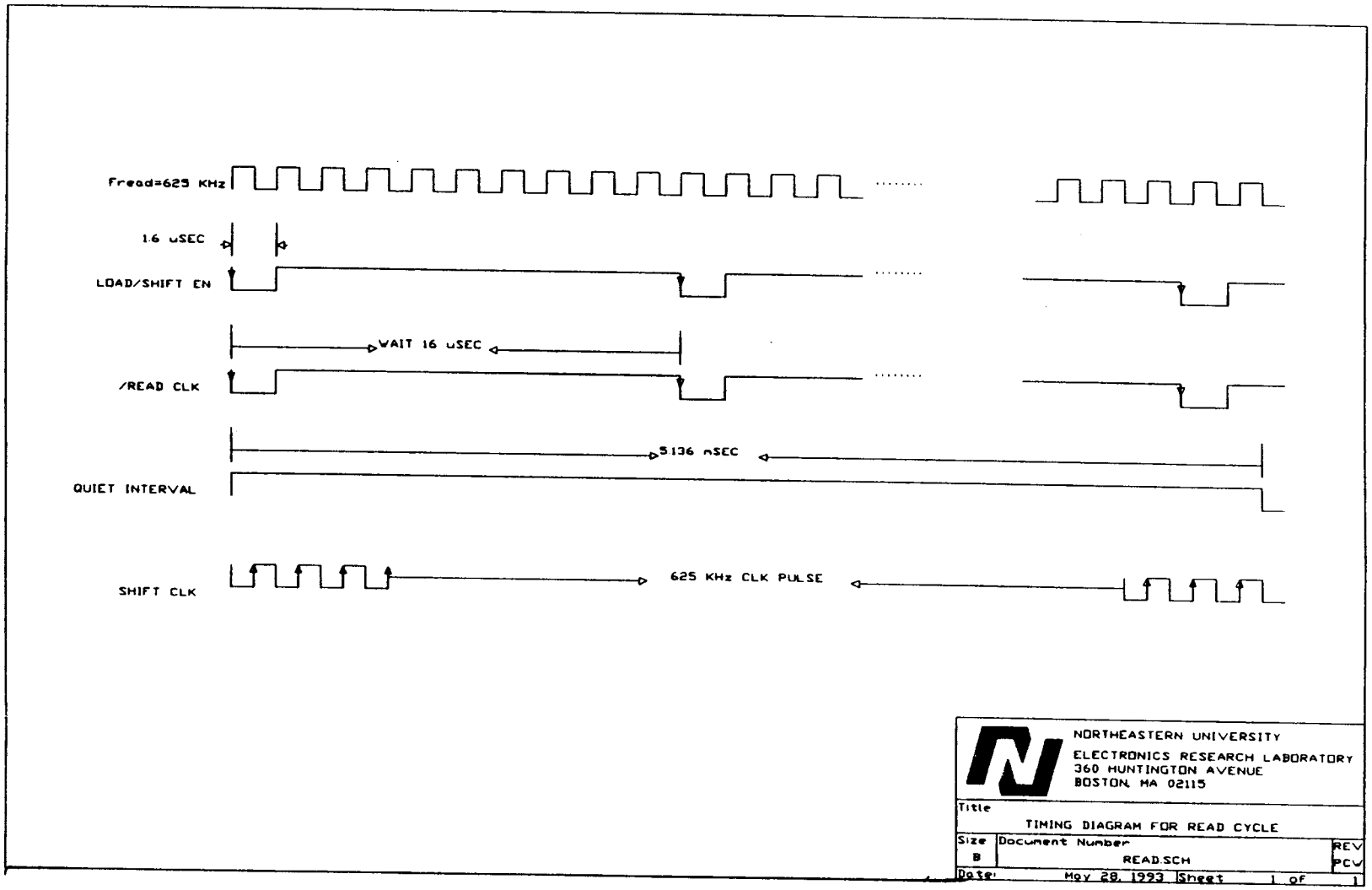


Figure 10. Timing Diagram for Reading Out Data From FIFO and Shifting Out Serial Bit Stream

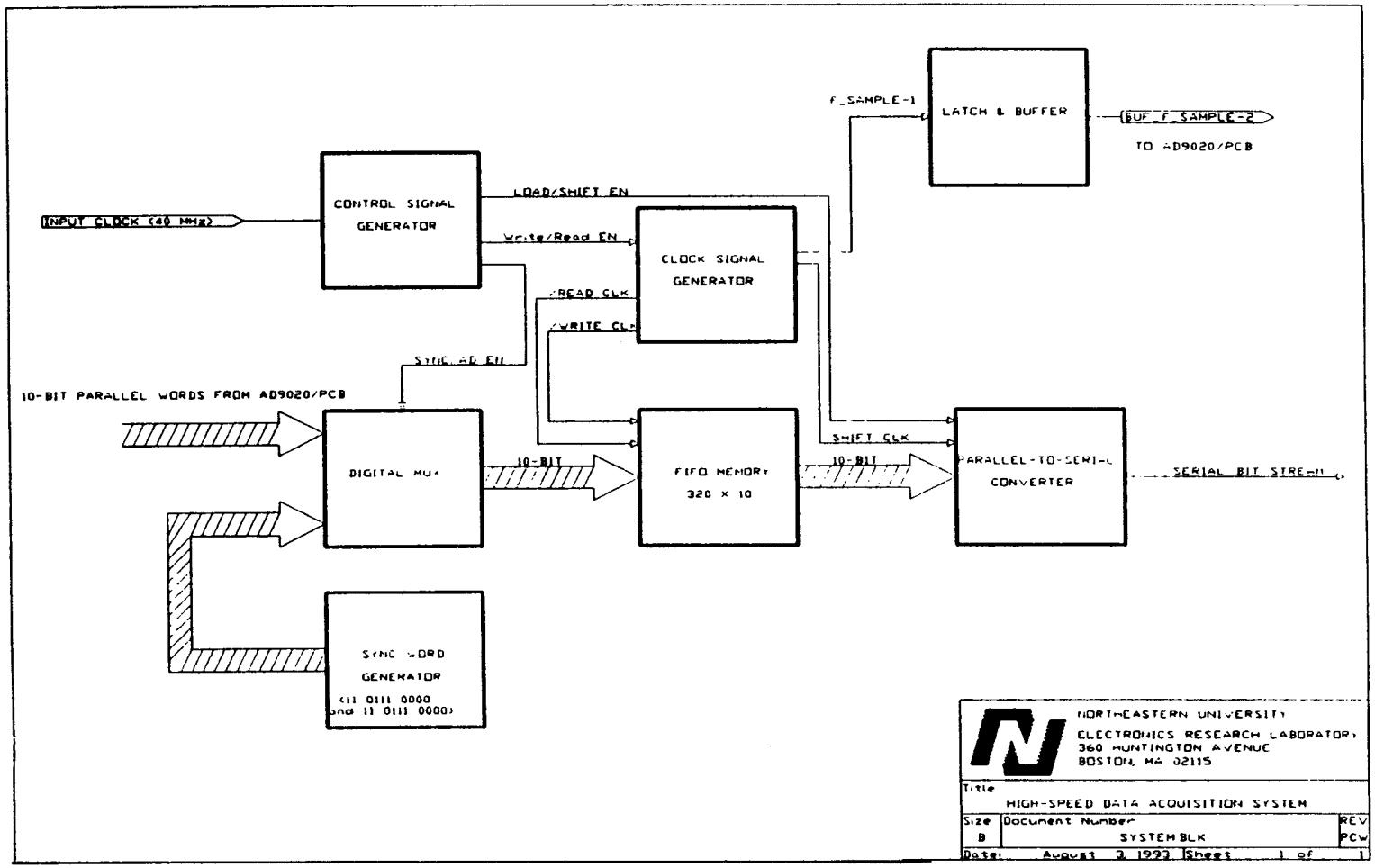


Figure 11. High-Speed FIFO Memory and Control Circuitry Block Diagram

Write/Read-Enable will initiate the reading of the parallel data from the FIFO memory. The Load/Shift-Enable initiates a load or shift operation for the parallel-to-serial converter circuitry. The SYNC/AD-Enable tells the system to insert two SYNC words from the SYNC word generator and to store all data from the AD9020/PCB thereafter.

The above circuitry described in this section was first incorporated onto a bread board. During testing, it was found that noise and glitches were present in the timing and control signals when the system was operating at 3 MHz and above. The noise and glitches were expected due to long leads and poor shielding in the circuit layout. In general, this bread board could only handle frequency ranging up to 1 MHz to 2 MHz. Since the system is operating at 20 MHz, a printed circuit board is required. This PCB must include the timing circuit, control cuits, FIFO memory, SYNC word generator, digital multiplexer and parallel-to-serial converter. The AD9020/PCB and the memory-and-control circuitry PCB can be easily interconnected.

The design of the printed circuit board is described in the following paragraph. A schematic diagram of the circuitry is generated by ORCAD computer-aided drafting software. Using the schematic diagram, a wire list of the design can also be generated through ORCAD. The wire list is then used to generate the printed circuit board layers by using AUTOPCB. The AUTOPCB is a computer-aided printed circuit design software used on a personal computer. The AUTOPCB uses the wire list of the design and the dimensionality

of the parts to generate a basic format layout for the printed circuit board. The layers of the printed circuit board are further re-edited by an ACAD computer-aided drafting software so that proper layout format is achieved. Figure 12 shows the silk screen of the printed circuit board. All the commponents on the PCB are approximately 0.25 inch apart. The dimension of the board is 7.7 inches x 6.6 inches. There are two layers on the board. Figure 13 shows the circuit side layer, whereas Figure 14 shows the component side layer. The interconnected wires (or traces) are 0.10 inch apart. The power and ground traces on both layers are 0.10 inch wide with 1 oz thick copper. The interconnected traces are low voltage and low current. Thus, they require 0.025 inch wide with 1 oz thick copper [7]. Once the re-editing is done using ACAD, the AUTOPCB is used again to generate the GERBER files. The GERBER files are used by many manufacturers to fabricate a printed circuit board. Since Pre-Mark Printed Circuit Inc quoted lower prices than other bidders, they were chosen to fabricate a printed circuit board.

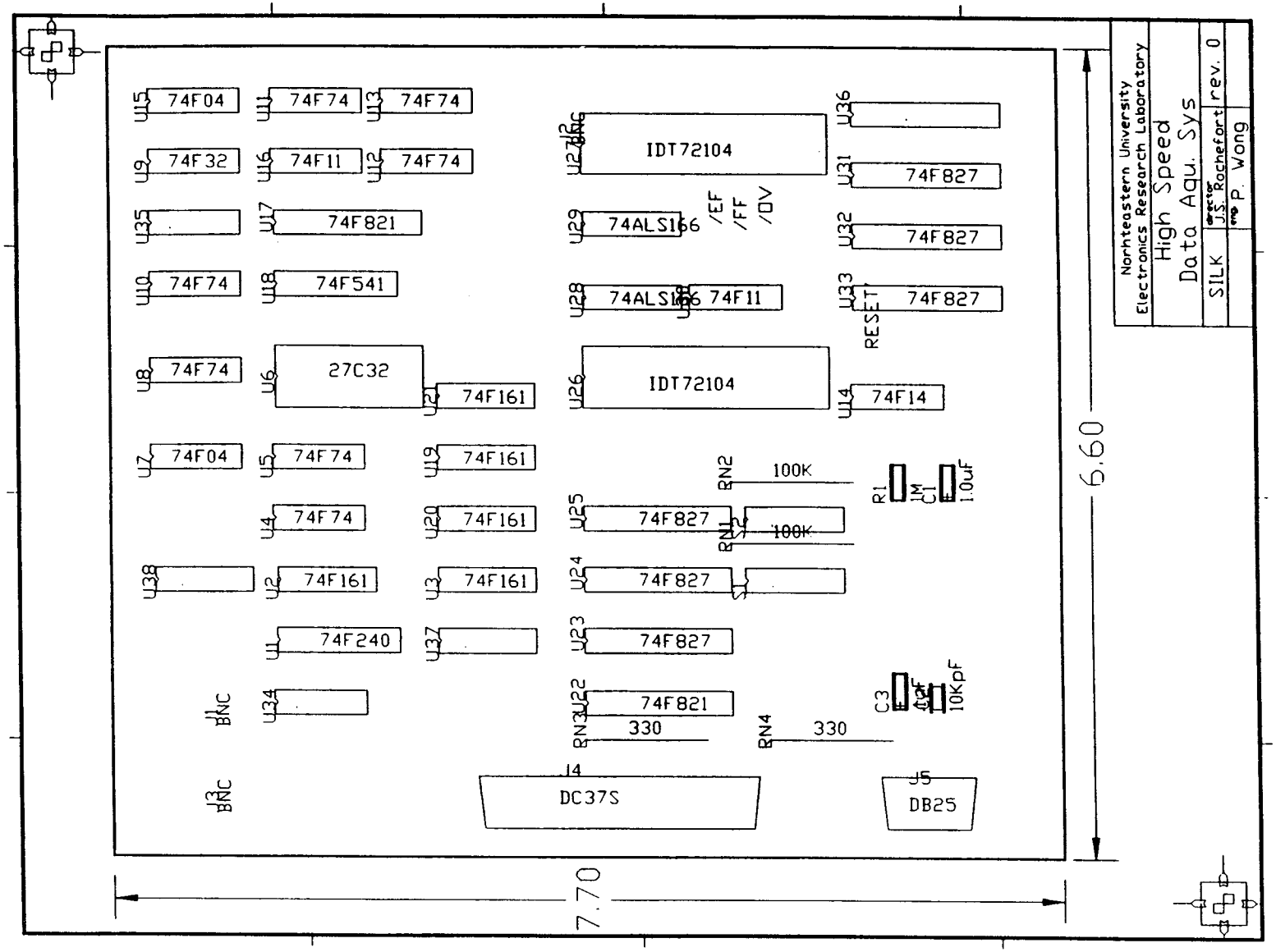


Figure 12. Silk Screen for the High-Speed FIFO Memory and Control Circuitry Printed Circuit Board

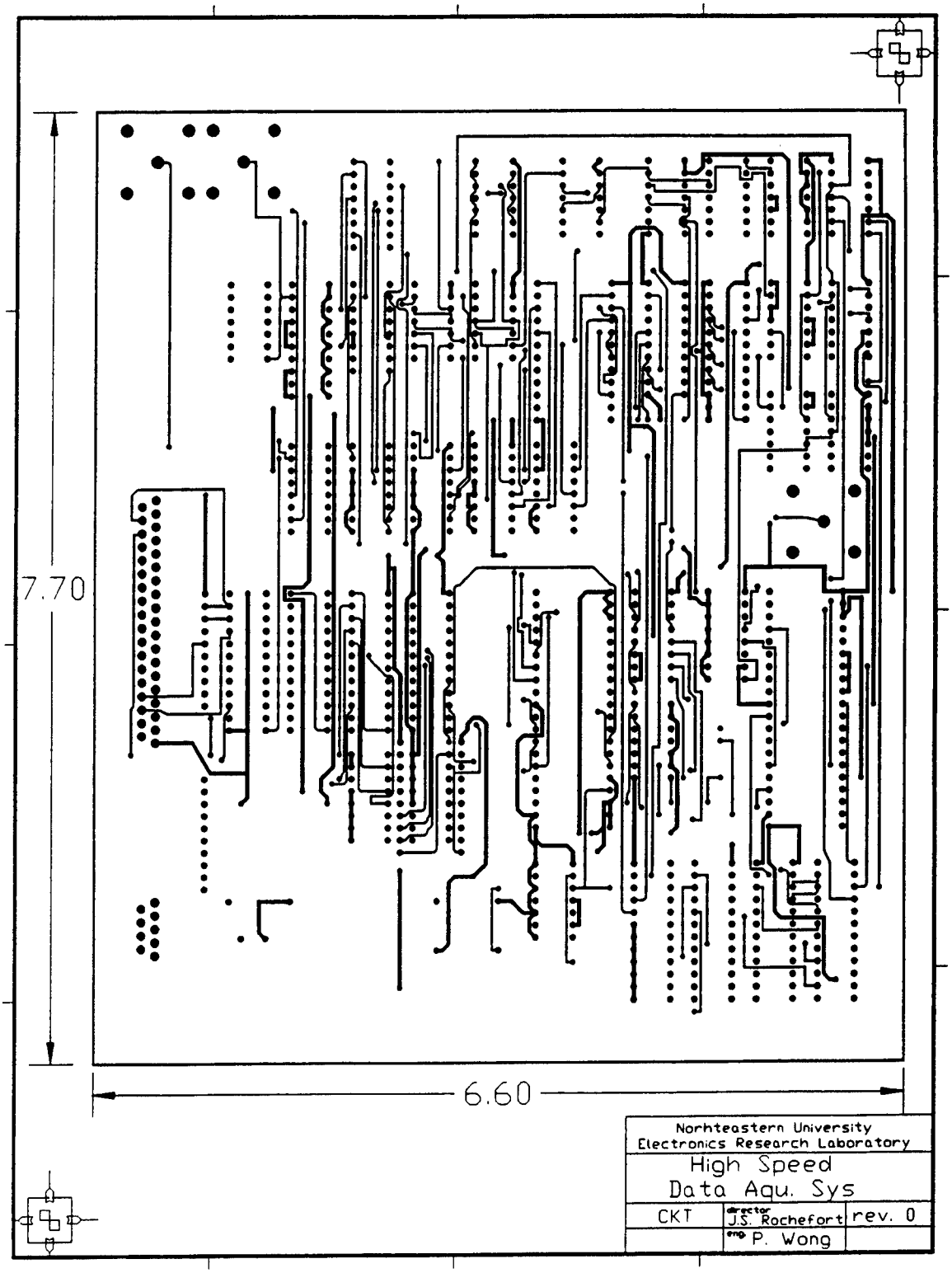


Figure 13. Circuit Side Layer for the High-Speed FIFO Memory and Control Circuitry Printed Circuit Board

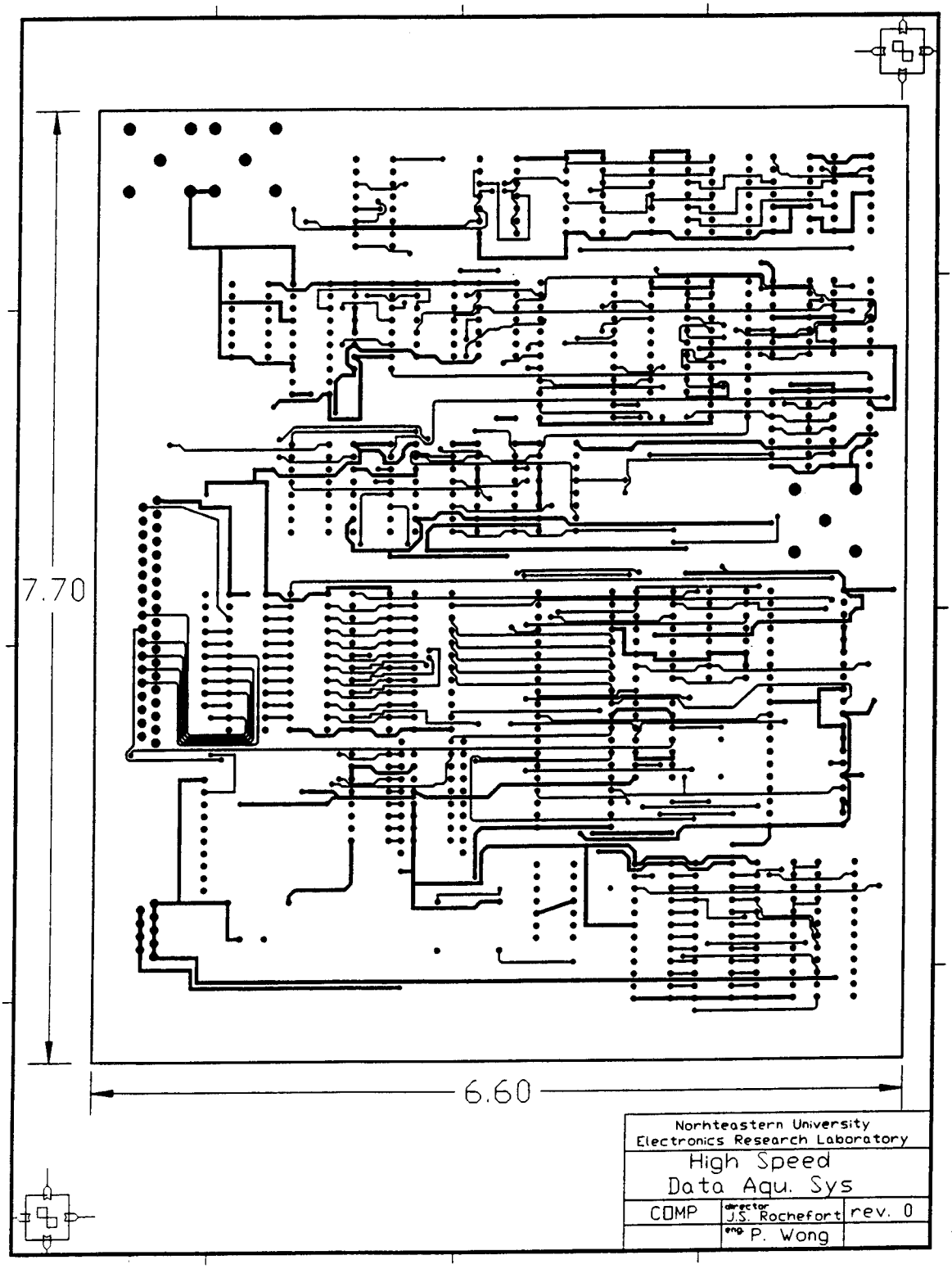


Figure 14. Component Side Layer for the High-Speed FIFO Memory and Control Circuitry Printed Circuit Board

5. EXPERIMENTAL RESULTS AND DISCUSSION

5.1 AD9020/PCB Evaluation Results

The AD9020/PCB evaluation board was tested by a DC linearity and a distortion test. All tests in this section were done using a WAVETEK clock generator to generate the sampling clock for the AD9020/PCB evaluation board. The sampling clock from the high-speed FIFO memory and control circuitry board was not used here. This ensured that the AD9020/PCB evaluation board was tested independently.

5.1.1 DC Linearity Test

Figure 15 shows the test setup for the DC linearity test. A DC signal was fed into the AD9020/PCB board. Using an oscilloscope/DVM, the DAC output of the evaluation board was measured. Table 1 shows a listing of tests at different input voltage levels and their percent error. For example, a 1.612Vdc input was fed into the AD9020/PCB, the output from the AD9020/PCB was approximately -0.04210Vdc. This output was obtained from the ADC to DAC of the AD9020/PCB. Since the output range of the AD9713 DAC from the AD9020/PCB can range approximately 0.0Vdc to -1.075Vdc, and the input range of the test can range from 1.75Vdc to -1.75Vdc, therefore, the DAC output can be approximated by the following equation:

$$\text{DAC output} = -0.5375 + \text{Input Voltage} * (1.075/3.5) \qquad (2)$$

A 1.612Vdc input will give a calculated value of -0.04239Vdc. The difference between the calculated value and the actual measured

value gave approximately 0.68% of error. As indicated from Table 1, the AD9020/PCB gave an overall percentage error of 0.7% within the capability of the test equipments.

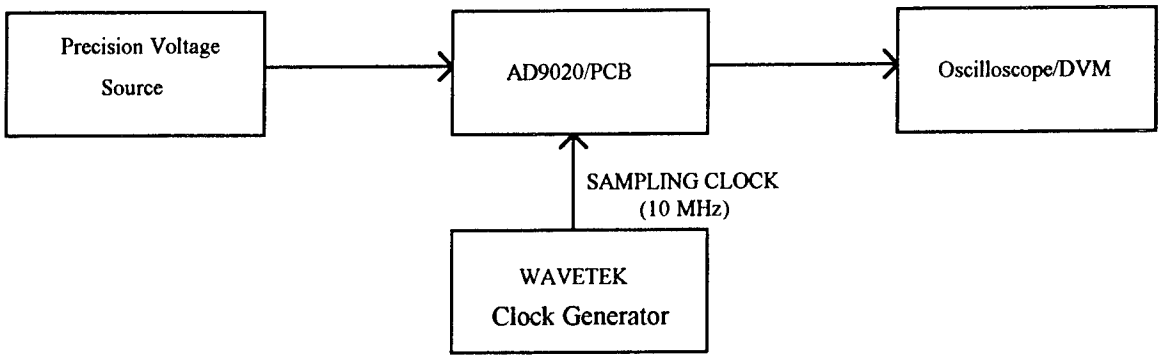


Figure 15. Linearity Test, Test Setup for AD9020/PCB

Table 1. DC Linearity Test Results for AD9020/PCB

Input Voltage	Test Result	Calculated Value	Percent of Error
1.612Vdc	-0.04210Vdc	-0.04239Vdc	0.68%
1.400Vdc	-0.1073Vdc	-0.10750Vdc	0.19%
1.000Vdc	-0.2313Vdc	-0.2304Vdc	0.39%
0.500Vdc	-0.3838Vdc	-0.3839Vdc	0.03%
-0.0002Vdc	-0.5369Vdc	-0.5376Vdc	0.13%
-0.500Vdc	-0.6869Vdc	-0.6911Vdc	0.60%
-1.000Vdc	-0.8388Vdc	-0.8446Vdc	0.69%
-1.400Vdc	-0.9673Vdc	-0.9675Vdc	0.02%
-1.612Vdc	-1.0254Vdc	-1.0326Vdc	0.70%

5.1.2 **Distortion Test**

For the distortion test, a sinusoidal signal was fed into the

AD9020 converter. The reconstructed signal was obtained from the circuitry of the ADC to DAC on the AD9020/PCB. This signal was fed into a HP333A distortion analyzer. Figure 16 shows the test setup. By using the distortion analyzer, the dynamic performance of the AD9020/PCB was measured. Since the equipment used on this test had not been calibrated for at least a decade, a calibration procedure was required. The test signal was first fed into a HP333A so that a distortion measurement was made. After this was done, the signal was then fed into the AD9020/PCB and another distortion measurement was made. The difference between the two measurements was approximately equal to the distortion value of the AD9020/PCB. For example, it was found that at 2V peak-to-peak sinusoidal input at 500 KHz gives approximately 0.5% of distortion. Figure 17 shows the test results of different test levels versus frequencies. The overall distortion was approximately within 0.55%. Once again, the percent distortion was assumed within the test equipment's capability.

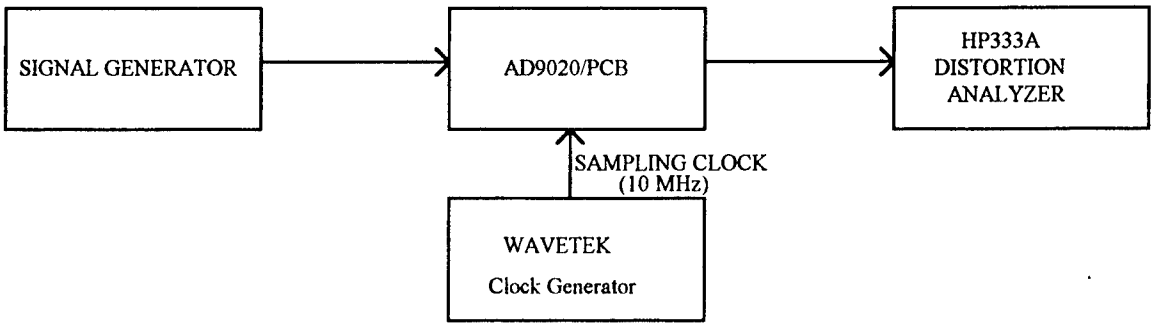
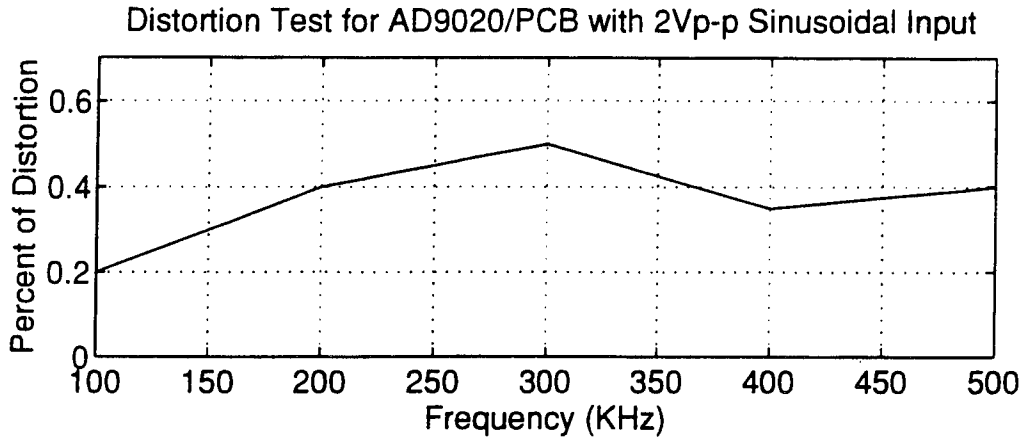
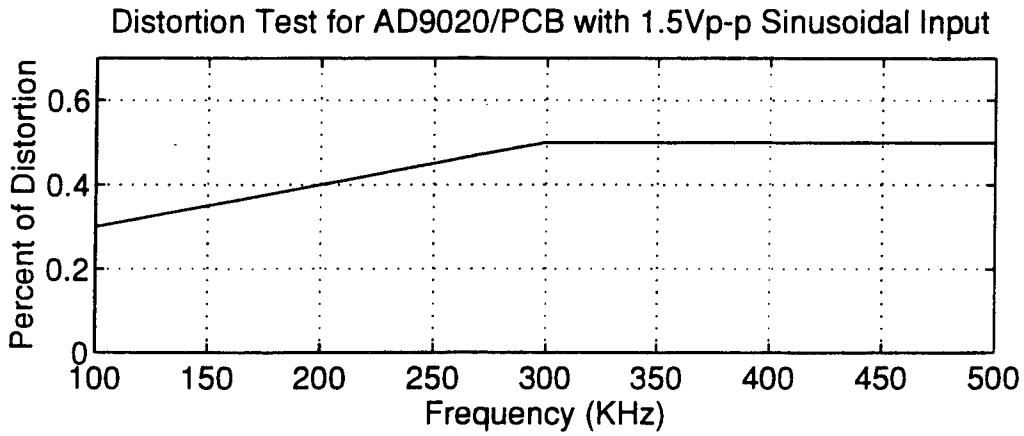


Figure 16. Distortion Test, Test Setup for AD9020/PCB





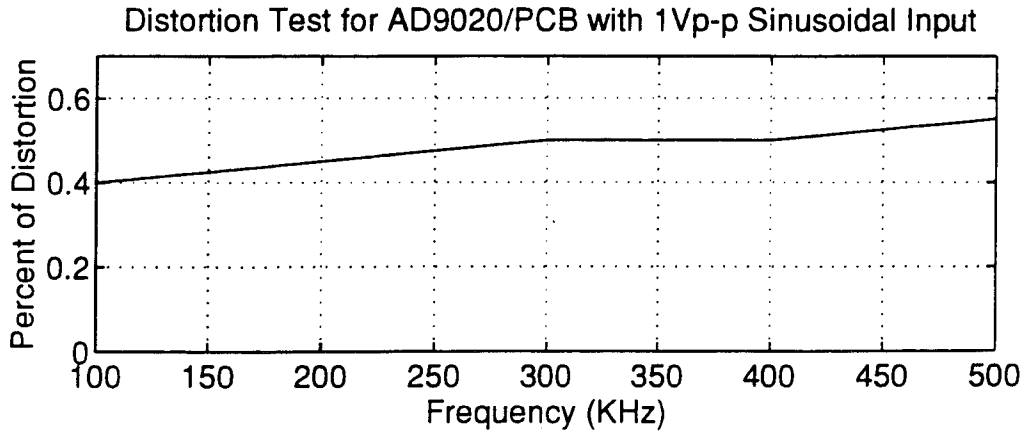


Figure 17. Distortion Test Results

5.2 Testing the High-Speed FIFO Memory/Control Circuitry PCB

The high-speed FIFO memory and control circuitry PCB were evaluated by walking a logic "1" through every memory location. This verified that all memory locations of the FIFO and control signals were operational. The test was performed without connecting the high-speed FIFO memory and control circuitry board to the 37-pin connector of the AD9020/PCB evaluation board. Since the high-speed FIFO memory and control circuitry board is capable of generating all required clocks and control signals, no external equipment was necessary. Only a SYSTEM 9000 was required to store its binary bit stream onto a hard disk. The SYSTEM 9000 is a computer-based bit synchronizer, decommutation, storage and data display unit which uses an AT bus on a personal computer (PC) [10]. It was designed by Terametrix Systems International, Incorporated.

The procedure of the test will be described in the following paragraph. All bits on the 37-pin connector were grounded except for the bit to be tested. Starting from the least significant bit (LSB), a digital word of 00 0000 0001 was used. This digital word was then stored into FIFO memory and converted to serial bit stream. The serial bit stream was stored into the SYSTEM 9000. The test continued onto the next LSB, and so forth, until the most significant bit (MSB) is tested. In other words, 00 0000 0001 through 10 0000 0000 were needed to test the high-speed FIFO memory and control circuitry board. Table 2 shows the test results of this board. For simplicity, two SYNC words are listed along with the first 10 words. A complete set of 320 words can be verified by

Table 2. Test Results for the High-Speed FIFO Memory and Control Circuitry Board

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	001	
04	001	
05	001	
06	001	
07	001	
08	001	
09	001	
0A	001	
0B	001	
0C	001	

(a)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	002	
04	002	
05	002	
06	002	
07	002	
08	002	
09	002	
0A	002	
0B	002	
0C	002	

(b)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	004	
04	004	
05	004	
06	004	
07	004	
08	004	
09	004	
0A	004	
0B	004	
0C	004	

(c)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	008	
04	008	
05	008	
06	008	
07	008	
08	008	
09	008	
0A	008	
0B	008	
0C	008	

(d)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	010	
04	010	
05	010	
06	010	
07	010	
08	010	
09	010	
0A	010	
0B	010	
0C	010	

(e)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	020	
04	020	
05	020	
06	020	
07	020	
08	020	
09	020	
0A	020	
0B	020	
0C	020	

(f)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	040	
04	040	
05	040	
06	040	
07	040	
08	040	
09	040	
0A	040	
0B	040	
0C	040	

(g)

Memory Location (Hex)	Content (Hex)	
01	370	} SYNC word
02	370	
03	080	
04	080	
05	080	
06	080	
07	080	
08	080	
09	080	
0A	080	
0B	080	
0C	080	

(h)

Memory Location (Hex)	Content (Hex)
01	370
02	370
03	100
04	100
05	100
06	100
07	100
08	100
09	100
0A	100
0B	100
0C	100

} SYNC word

(i)

Memory Location (Hex)	Content (Hex)
01	370
02	370
03	200
04	200
05	200
06	200
07	200
08	200
09	200
0A	200
0B	200
0C	200

} SYNC word

(j)

the display on the SYSTEM 9000. This test did verify that the data words were stored into memory and converted into serial bit stream. For example, in Table 2(f), a digital word of 00 0010 0000 was used. The SYSTEM 9000 did store, reformat and display the two SYNC words and 00 0010 0000 digital words afterwards.

5.3 **System Integration Test**

The system integration test was used to test the complete system which consists of the AD9020/PCB and high-speed FIFO memory and control circuitry board. The system integration test consists of the system DC linearity and dynamic performance test. All tests in this section were performed using a 20 MHs sampling clock and a serial bit stream output at a rate of 625 KHz.

5.3.1 **System DC Linearity Test**

In the DC linearity test, a DC signal was fed into the AD9020/PCB. During the burst interval (or window) of 16.0 μsec, the AD9020/PCB converted the incoming signal into 10-bit parallel

words. The 10-bit parallel words were then stored into the high-speed FIFO memory and control circuitry board simultaneously. Once the window closed, the high-speed FIFO memory and control circuitry board stopped storing the incoming data. The parallel data were converted to serial bit stream. The serial bit stream was then clocked out at a rate of 625 KHz. The SYSTEM 9000 searched the correct SYNC words (11 0111 0000 and 11 0111 0000) to find the beginning of the frame. Once the SYNC words were found, the SYSTEM 9000 stored the two SYNC words and the reamining 318 words onto its hard disk. This process continued onto the next frame. Figure 18 shows the test method.

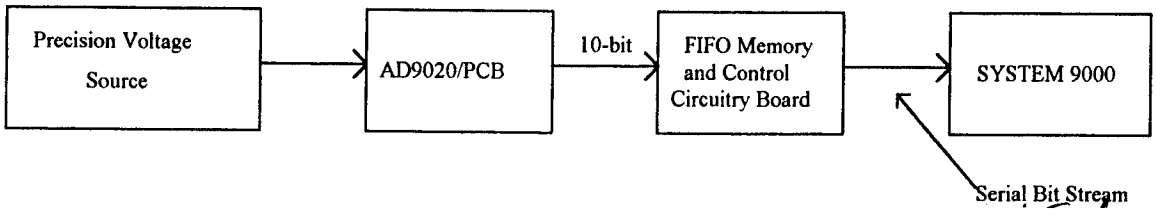


Figure 18. DC Linearity Test, Test Setup for Integrated System

Once the data was properly reformatted in SYSTEM 9000, the reconstructed signal was displayed using DADISP or MATLAB software packaging programs. Figure 19(a) shows a set of test results with input ranging from +1.75Vdc to 0.0Vdc. Figure 19(b) shows another set of test results with the input ranging from -1.75Vdc to 0.0Vdc. The test values in the figure were chosen arbitrarily. For example, in Figure 19(a), the input voltage at +1.75Vdc gave

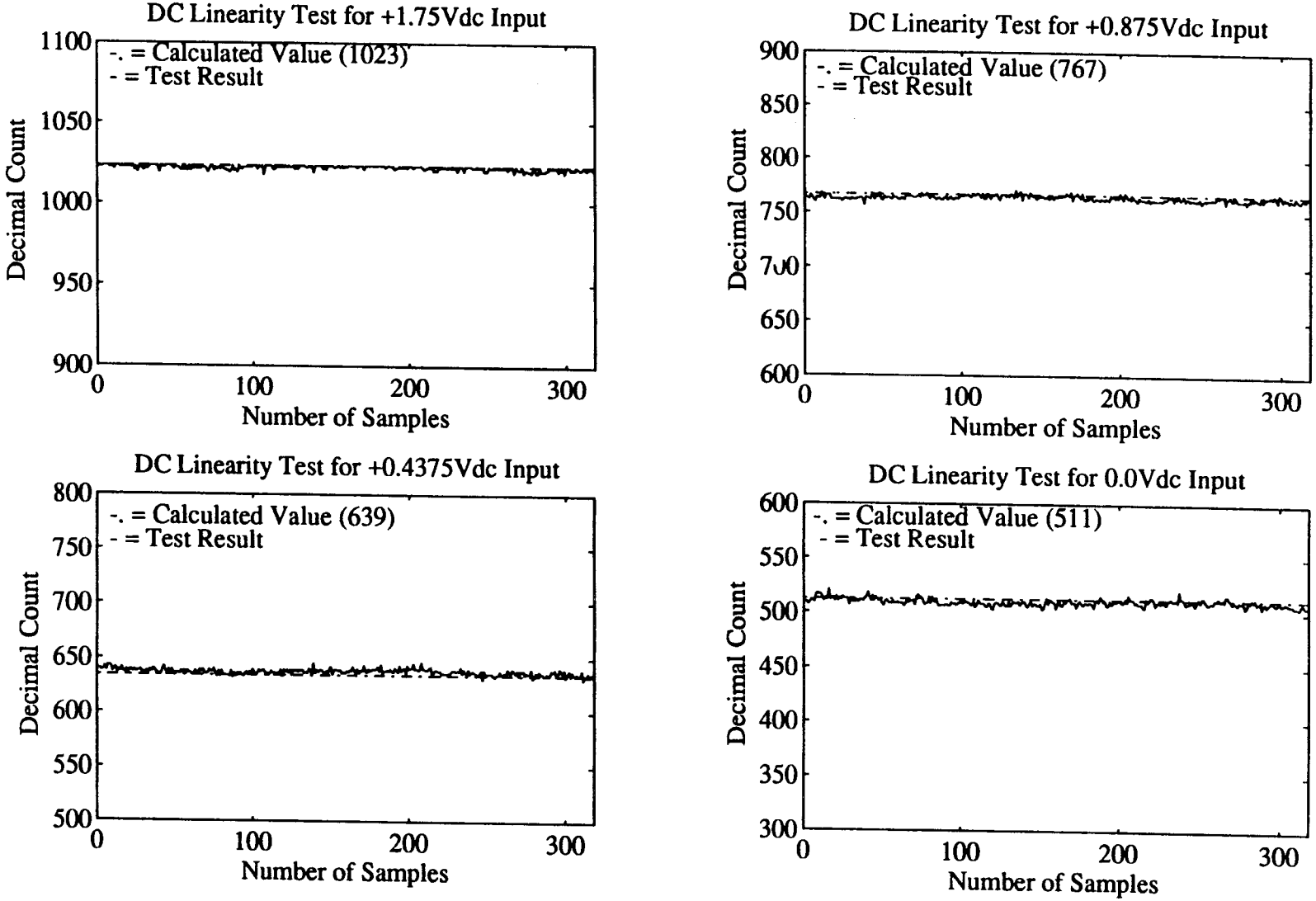


Figure 19(a) Integrated System Test Results for DC Linearity Test

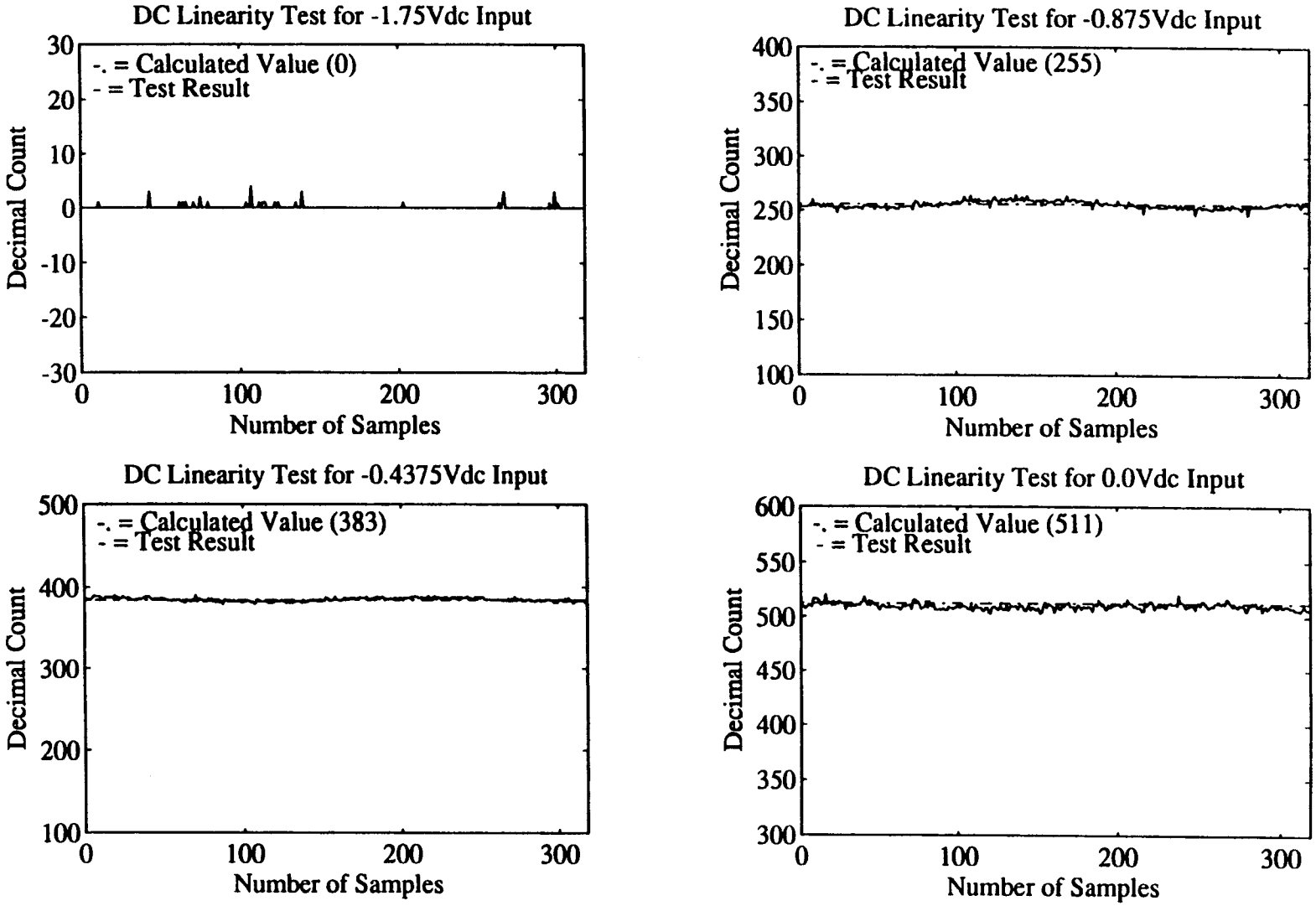


Figure 19(b) Integrated System Test Results for DC Linearity Test

approximately 1022 decimal count. The actual value is calculated as 1023 (decimal count). By assuming the system is linear, this value can be calculated using the following equation:

$$\text{Decimal Count} = (\text{Input Voltage})^{*}(511.5/1.75)+511.5 \qquad (3)$$

where the Decimal Count denotes the decimal representation of the analog-to-digital conversion. Thus, the test verified the linearity of the system. Figure 20 shows the linearity plot of the system. All the data points in this graph were calculated by averaging each individual test of Figure 19. The test results from Figures 19 and 20 show the system have a percent error with 0.1%.

5.3.2 **System Dynamic Performance**

The dynamic performance test for the integrated system was performed similarly to the DC linearity test as mentioned above. The only difference is the periodic signals and complex signals being used as an input source to the system. The SYSTEM 9000 was also being used here to decommutate and store the serial bit stream onto the hard disk, so further analysis of the data could be done. Since, the signals were periodic or complex, the peak amplitude value of the signal was once again calculated using Equation (3).

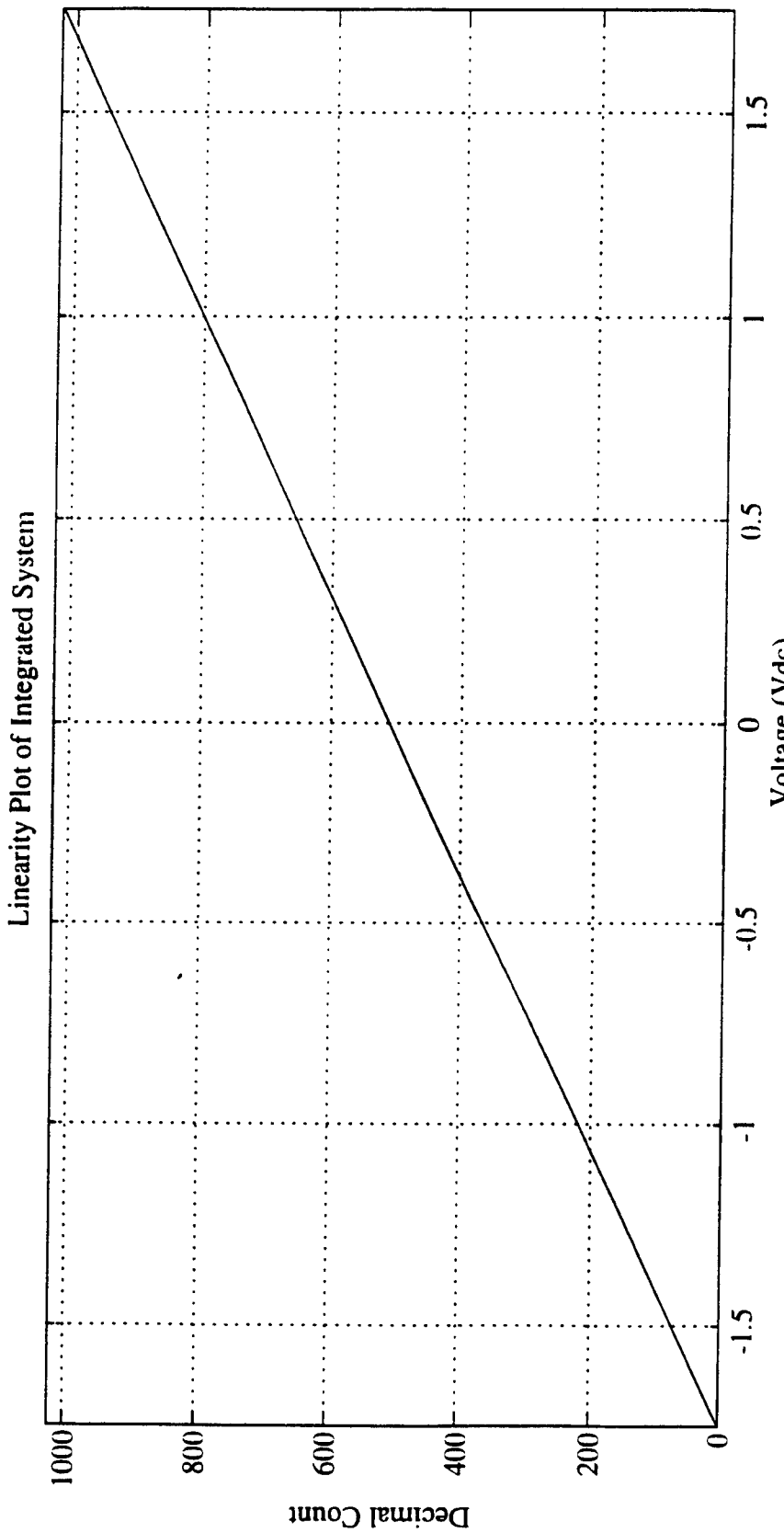


Figure 20. Linearity Plot

5.3.2.1 System Dynamic Performance With Periodic Signal

The first set of this test was performed here by applying a 3.5V peak-to-peak periodic input signal at 1 MHz to the system. The following periodic signals used here were: sinusoidal, triangular, and square signals. The positive peak value of the periodic signal must give a decimal count of 1023, and the negative peak value must give a decimal count of zero. Figure 21(a) shows the reconstructed signal for 3.5V peak-to-peak 1 MHz sinusoidal test signal. Point A1 in the figure shows the decimal count for the positive peak value, whereas point B1 in the same figure gives the decimal count of the negative peak value. Figure 21(b) shows the spectrum of Figure 21(a). The spectrum plot was plotted by using the Fast Fourier Transform (FFT) built in function in MATLAB Point f1 shows the cutoff frequency at 3134.8 Hz of Figure 21(a). In order to compare the reconstructed signal frequency to the original input signal frequency, the reconstructed signal frequency must be multiplied by a factor of 320. This gives the following results:

$$320 \times 3134.8 = 1.003136 \text{ MHz} \qquad (4)$$

1.003136 MHz gives approximately 0.3% of error compared to the original input sinusoidal frequency. As indicated from Figure 21, the reconstructed signal from the SYSTEM 9000 gave approximately the same result of the original signal with a factor of 320 difference. These results indicated the system did convert and store its data properly with percent error within 0.3%.

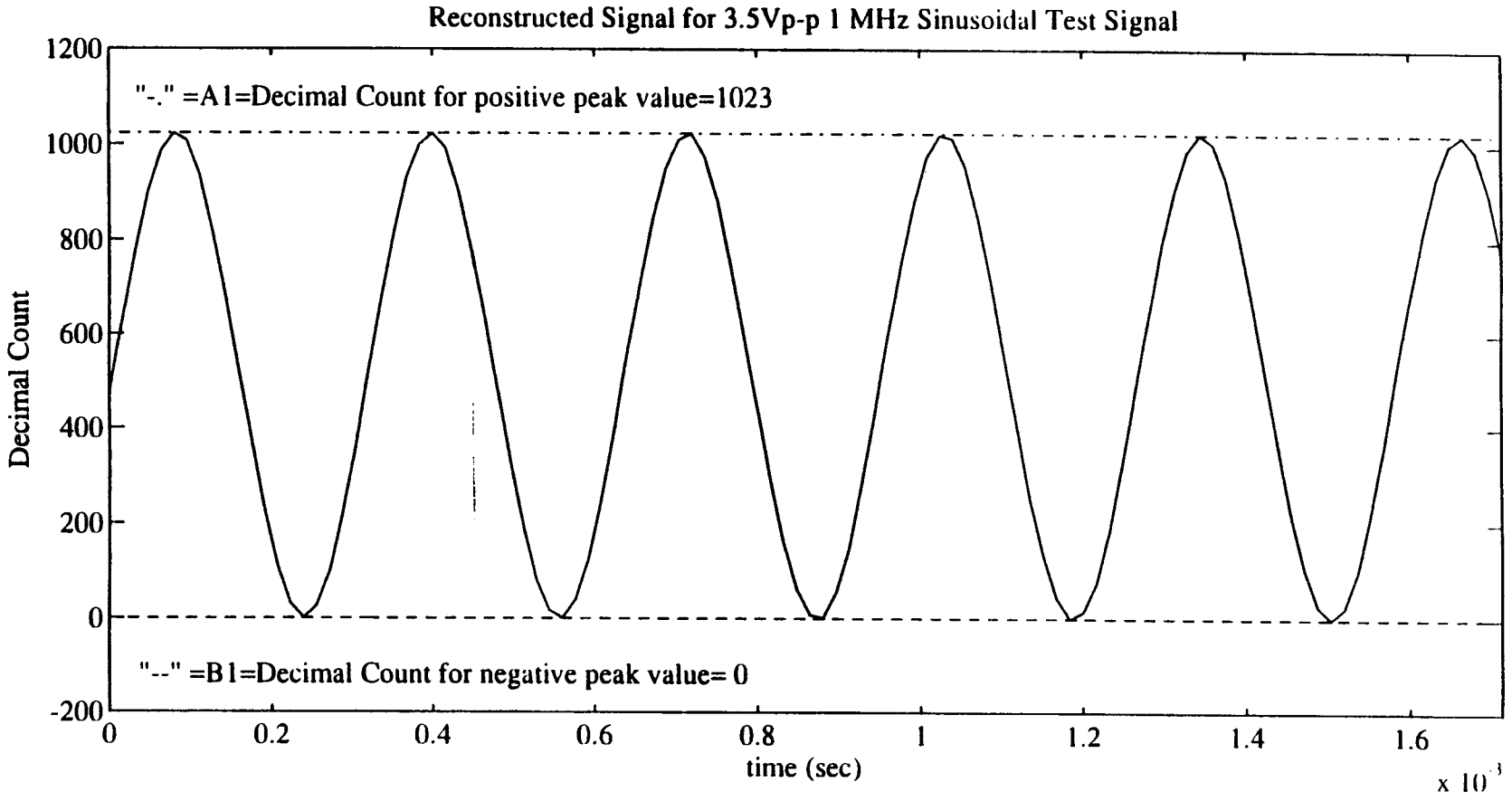


Figure 21(a) Reconstructed Signal for 3.5Vp-p 1 MHz Sinusoidal Test Signal

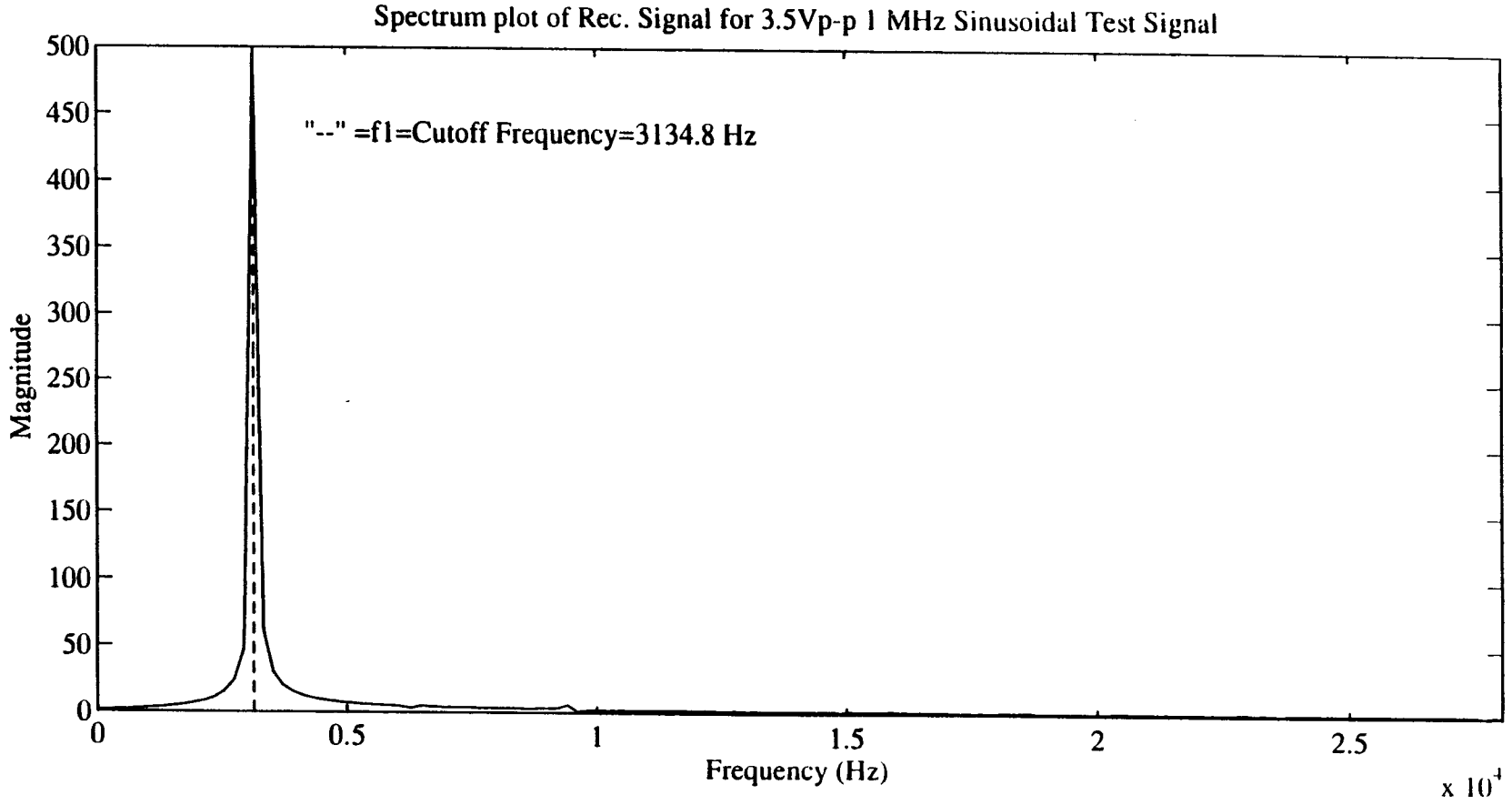


Figure 21(b) Spectrum Plot for 3.5Vp-p 1 MHz Sinusoidal Test Signal

Figure 22(a) and (b) show the results of the triangular signal at 3.5V peak-to-peak 1 MHz. The verification of the original signal can be done as follows:

```
Point f2 = 3134.8     <== 320 x 3134.8 = 1.003136 MHz
Point A2 = 1023       <== Decimal Count for positive peak value

Point B2 =  0         <== Decimal Count for negative peak value
```

For the square signal, a similar verification of the original signal can be verified as mentioned above. The result is shown in Figure 23. Once again, the verification can be done as follows:

```
Point f3 =  3134.8      <== 320 x 3134.8      = 1.003136 MHz
Point A3 = 1023         <== Decimal Count for positive peak value

Point B3 = 0            <== Decimal Count for negative peak value
```

Figures 24 and 25 show another set of test results at different test levels and frequencies.

Overall, these test results indicated the system works well for periodic signals with different frequencies and amplitudes. These results also indicated that the accuracy of the system is within 0.3% of error.

5.3.2.2 **System Dynamic Performance With Complex Signal**

The complex signal performance test for the integrated system was done by using complex signal generated through a PHILIPS PM 5715 pulse generator. To simulate the output of an instrument, the PHILIPS PM 5715 was configured so that when the window was opened the PM 5715 would be triggered. Once the PM 5715 was

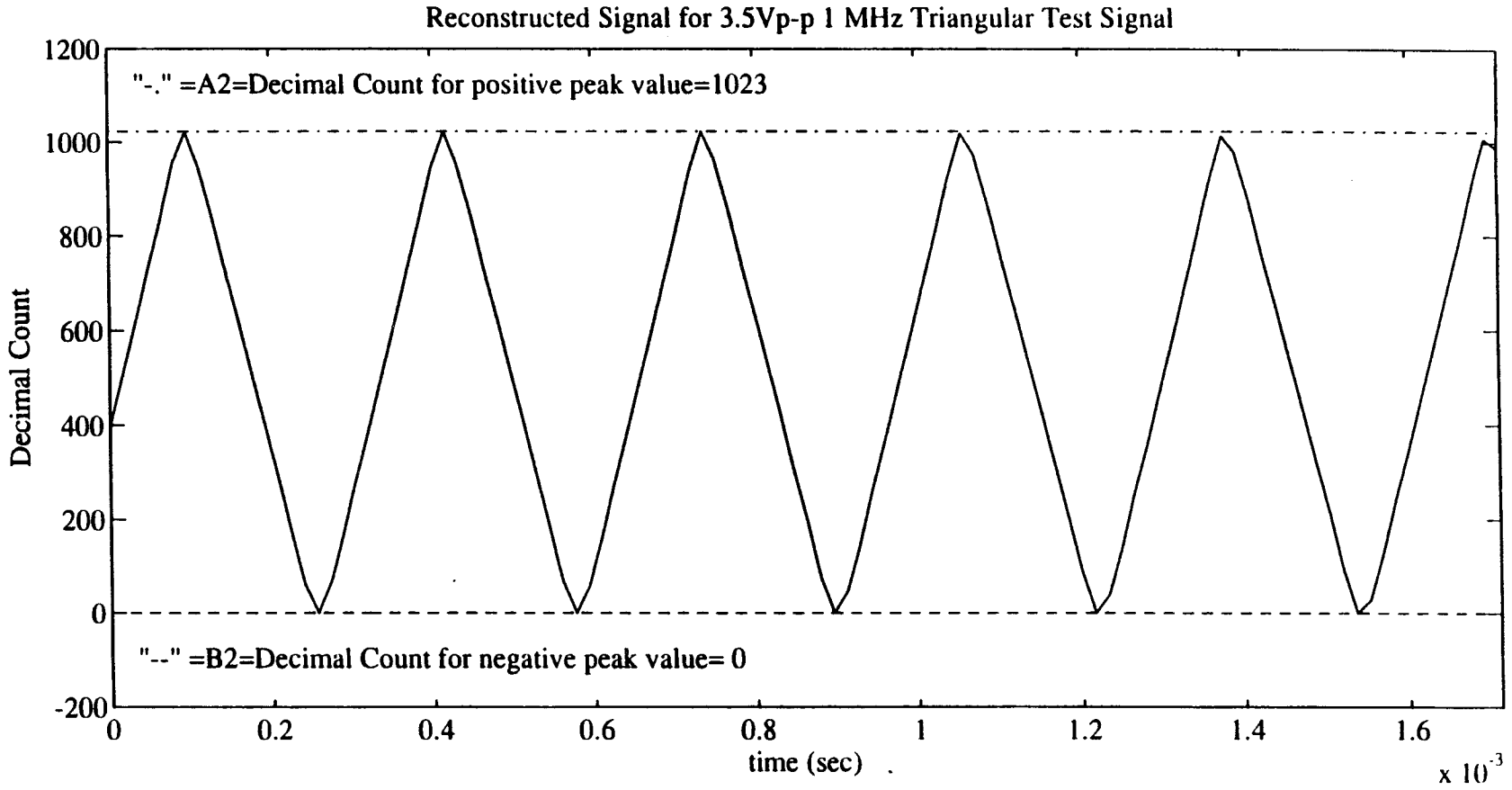


Figure 22(a) Reconstructed Signal for 3.5Vp-p 1 MHz Triangular Test Signal

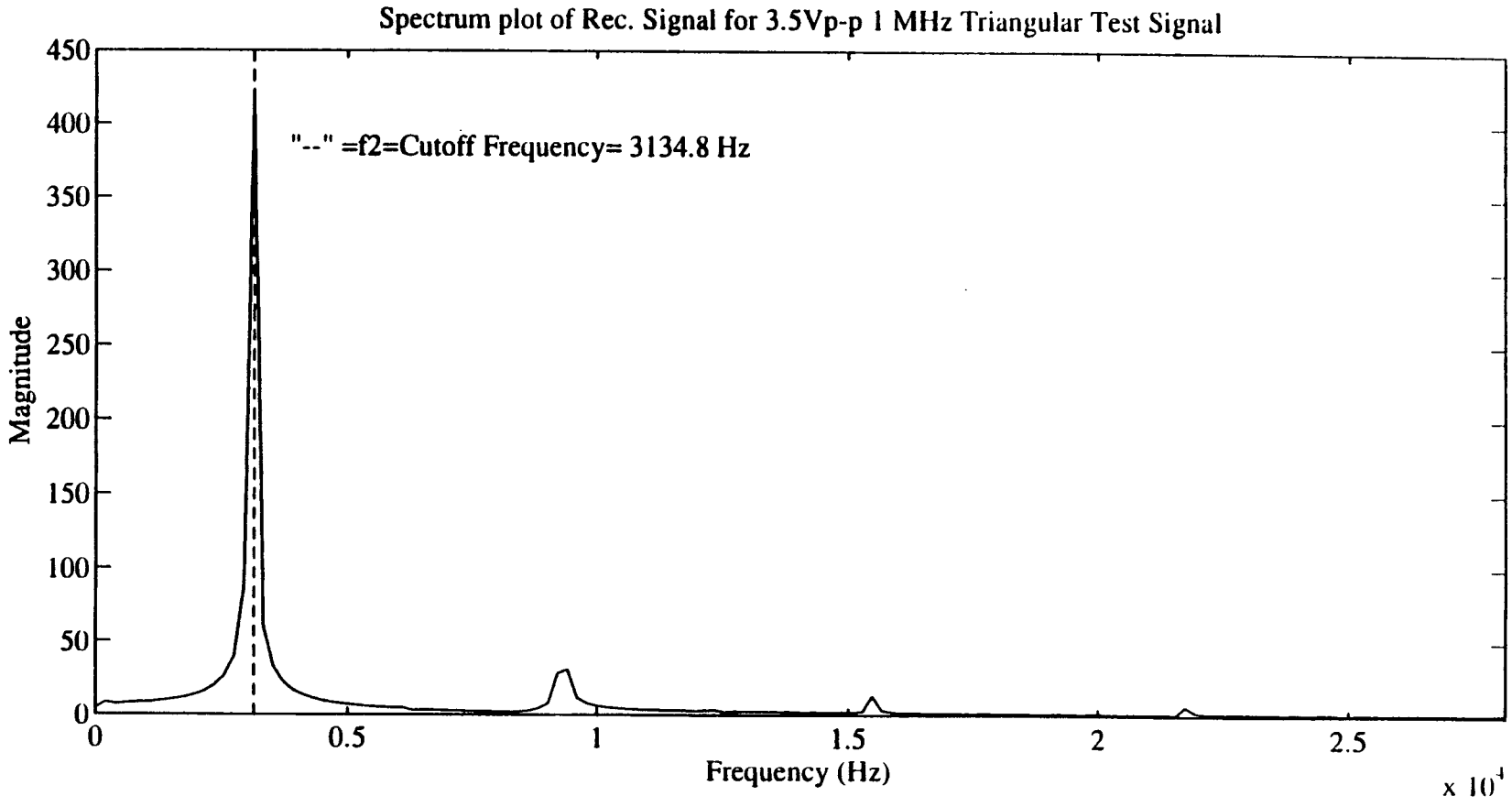


Figure 22(b) Spectrum Plot for 3.5Vp-p 1 MHz Triangular Test Signal

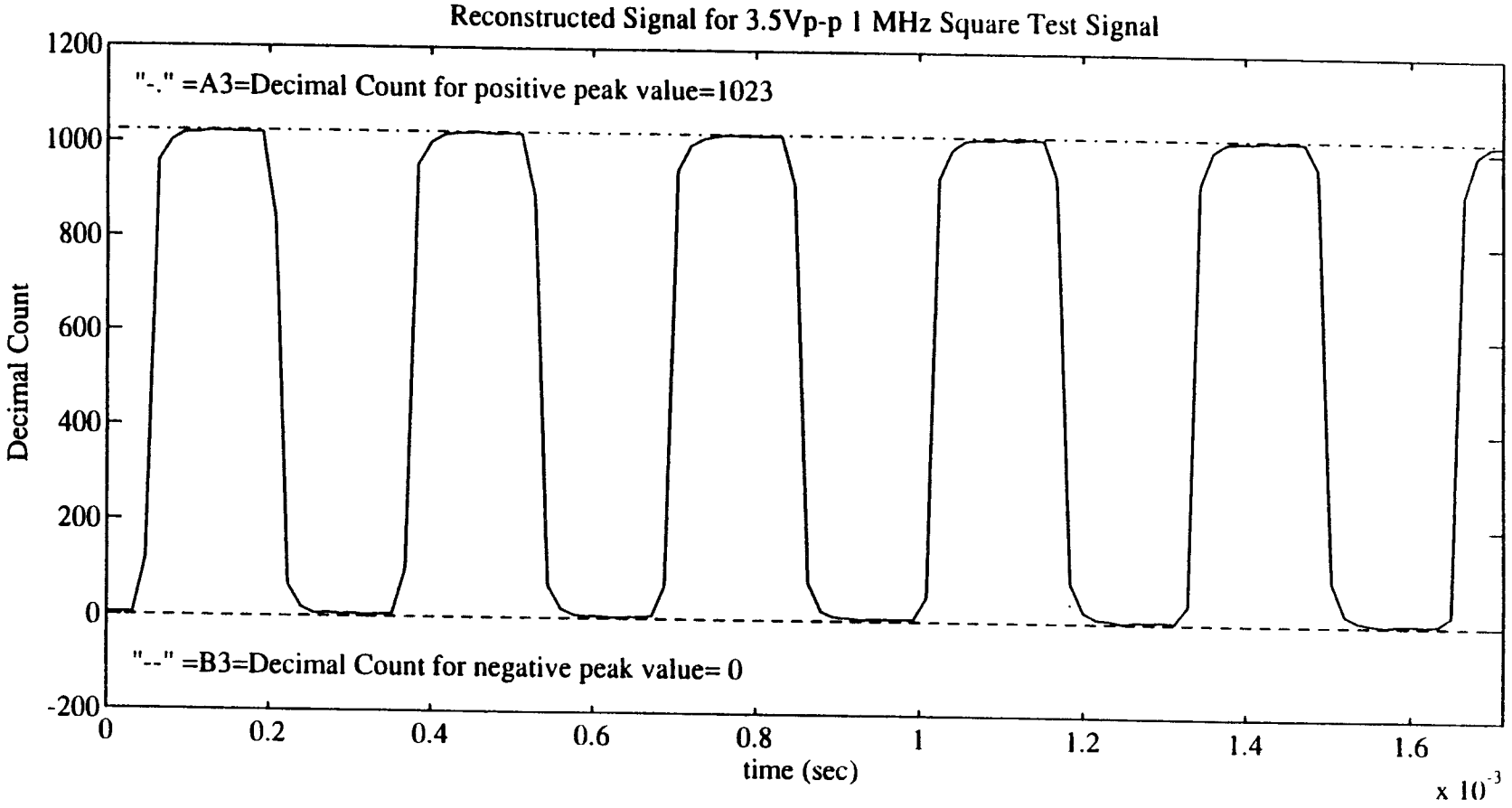


Figure 23(a) Reconstructed Signal for 3.5Vp-p 1 MHz Square Test Signal

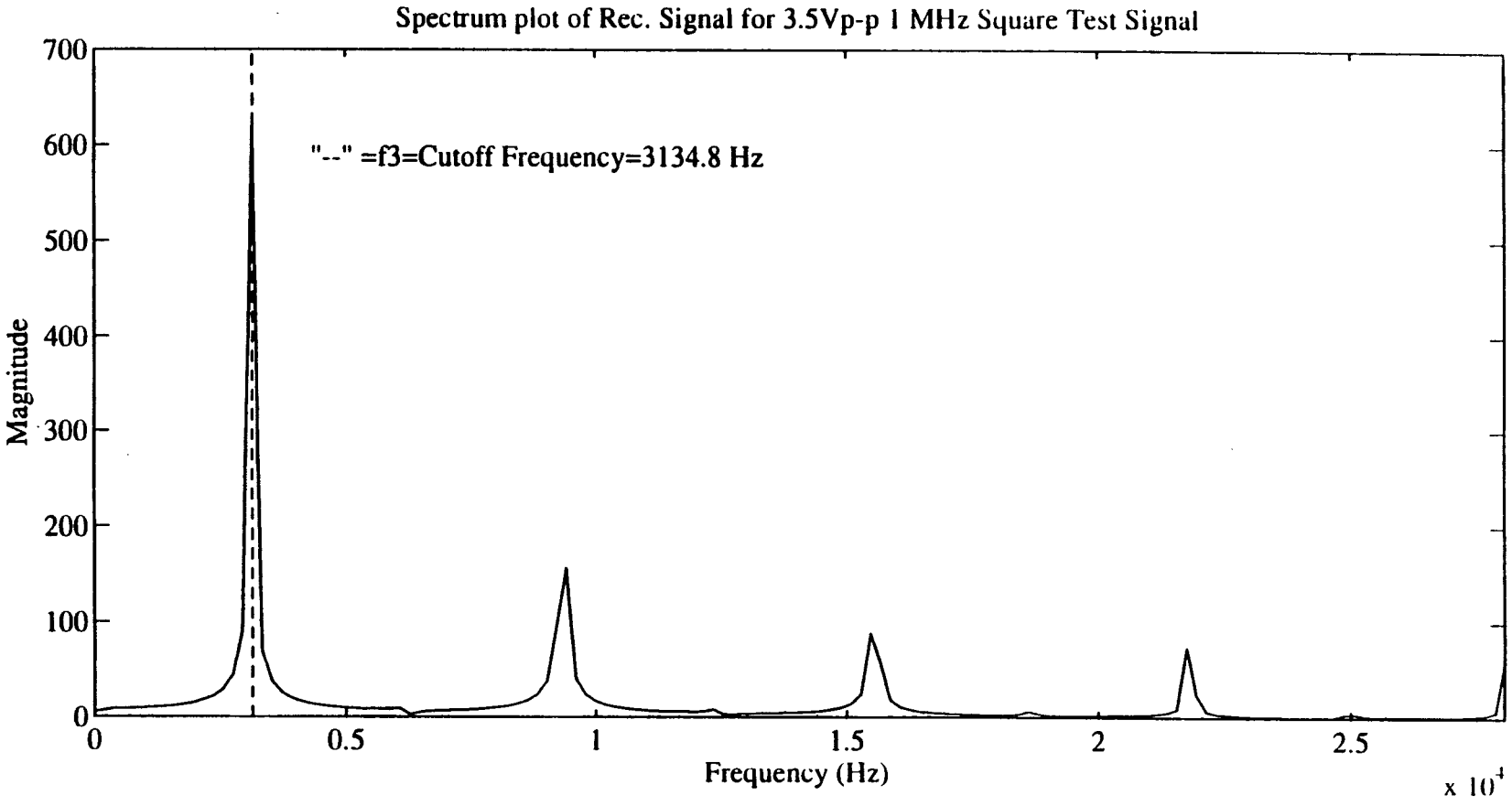


Figure 23(b) Spectrum Plot for 3.5Vp-p 1 MHz Square Test Signal

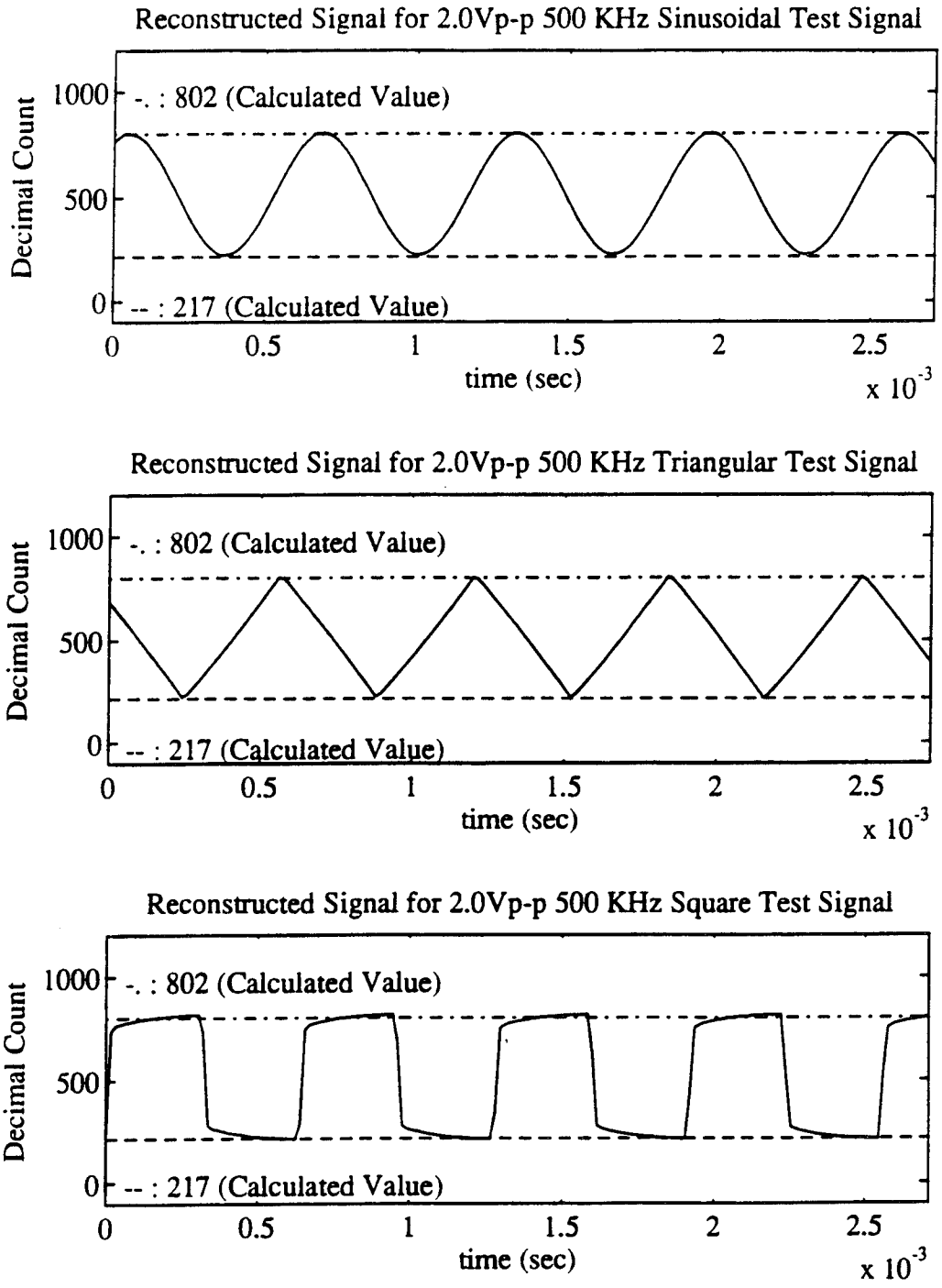


Figure 24. Reconstructed Signal for 2.0Vp-p 500 KHz Periodic Test Signals

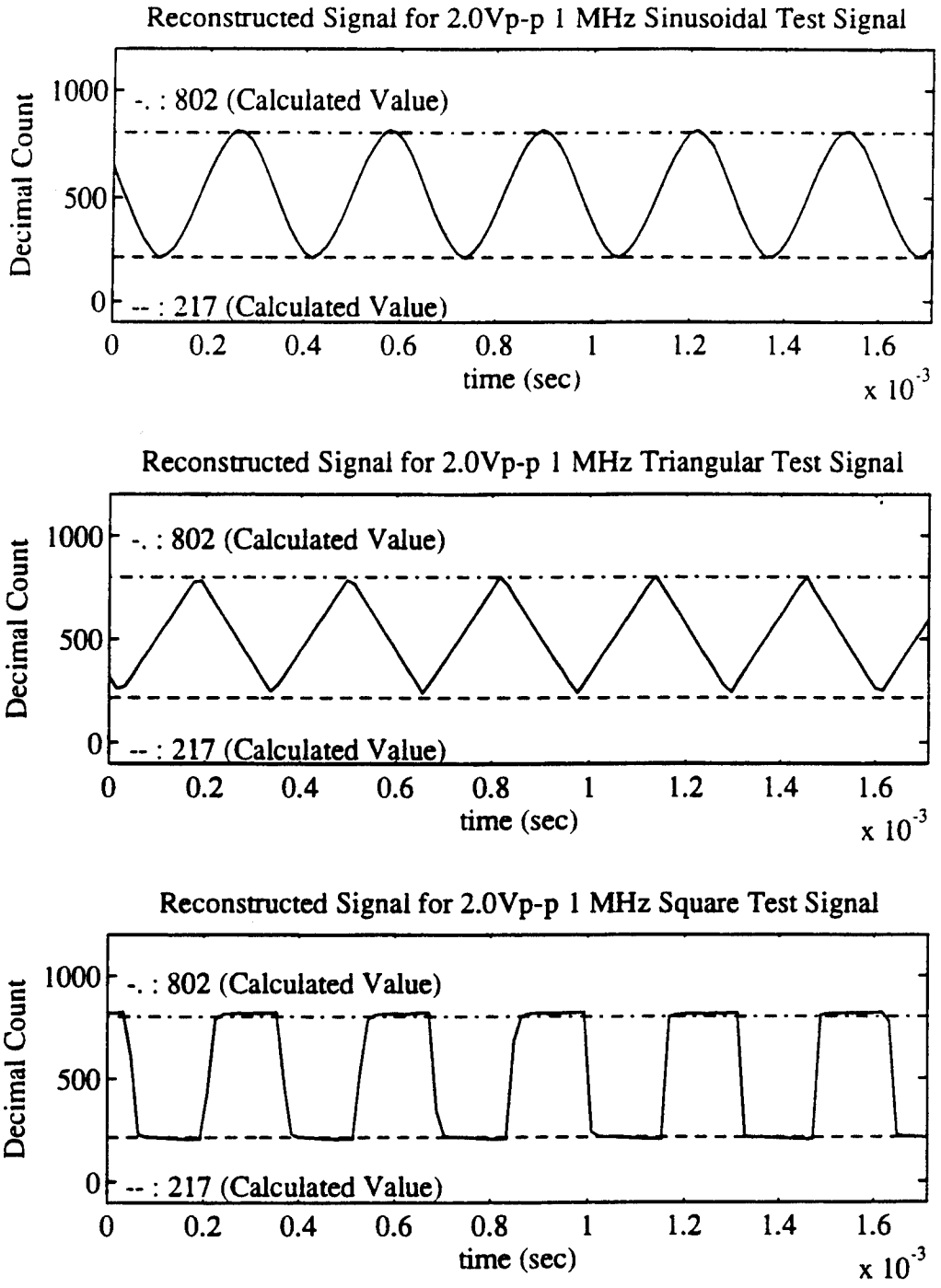


Figure 25. Reconstructed Signal for 2.0Vp-p 1 MHz Periodic Test Signals

triggered, the PM 5715 produced a pulse with very fast rise and fall time. It could also generate a pulse width to meet specified test requirements. The PM 5715 also has an option to generate pulse with delay time. Figure 26 shows the test setup for a complex signal test.

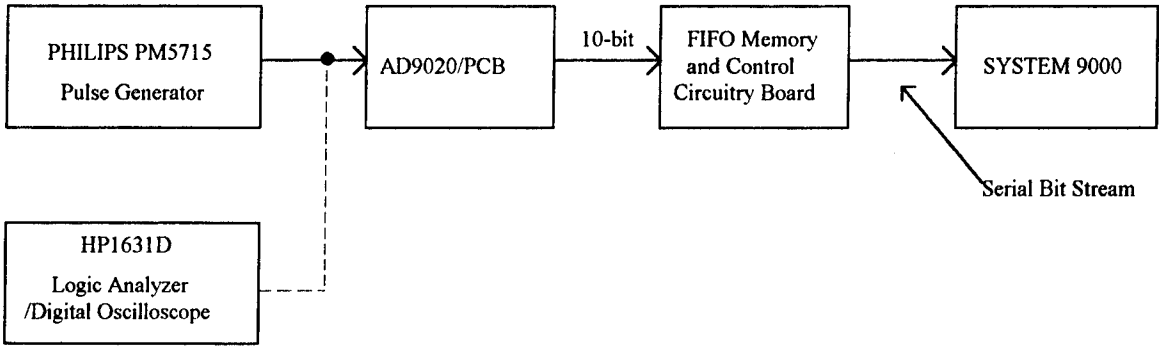
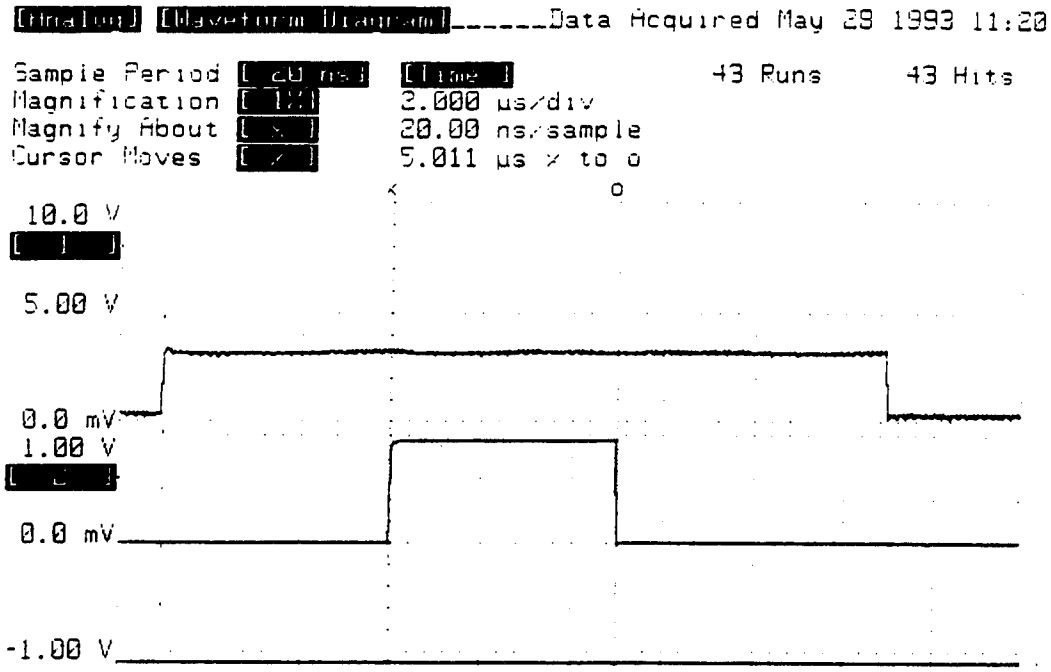
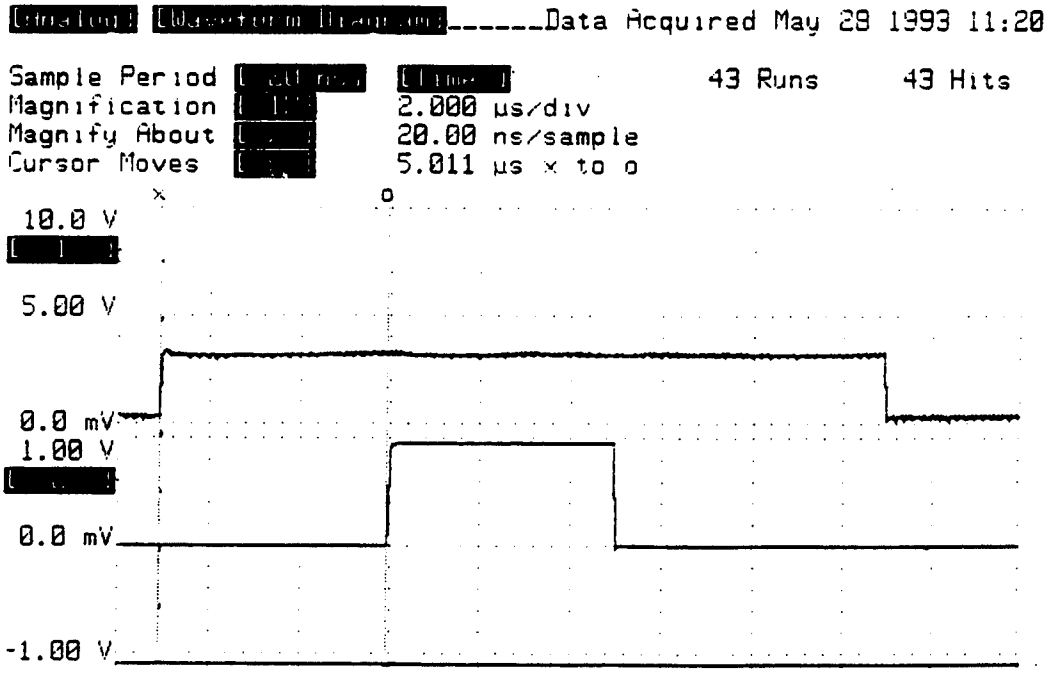


Figure 26. Complex Signal Test, Test Setup

Using a HP1631D logic analyzer/digital oscilloscope, the input signal could be captured and printed for verification against the stored signal on the SYSTEM 9000. Figure 27 shows the printout of a complex signal tested on the integrated system. Figure 27(a) shows the pulse width of the test signal which was approximately 5.011 μsec as indicated from time X to time O in the figure. Figure 27(b) shows the signal was delayed for 5.011 μsec before the pulse was initiated. Time X to time O indicates this value. The values of Figure 27(a) and (b) were chosen arbitrarily. Once the serial bit stream of the integrated system was stored into the SYSTEM 9000, the data was reconstructed and displayed on MATLAB. Figure 28 shows the reconstructed signal of Figure 27. In Figure



(a)



(b)

Figure 27. Channel 1 Indicates the Burst Interval of 16.0 µsec, whereas Channel 2 Indicates Test Signal Waveform

28, the interval Xd shows the time delay of the reconstructed signal. For verification of the original signal, a factor of 320 must be divided. This gives approximately 5.00 usec. At interval Xw, the values reads 1.59 msec. Once again, to verify the reconstructed signal a factor of 320 was divided. This gives approximately 4.97 μsec. The results of Figure 28 shows the system has an accuracy within 0.8% of error. A slower rise and fall time signal was used for the next test.

Figure 29 shows the test signal waveform. The waveform has a rise time of 1.88 μsec and a fall time of 5.04 μsec as indicated by time X to time O in the figure. The SYSTEM 9000 was used to analyze the reconstructed waveform. Figure 30 shows the test result of Figure 29. Xr was given as the rise time of the reconstructed waveform. Xr was approximately equal to 600 msec. Thus, Xr divided by 320 (Xr/320 = 1.875 msec) gave the rise time value of the original signal with a percent error of 0.27%. A similar comparison was also done on Xf, the fall time of the reconstructed waveform. Xf divided by 320 (Xf/320 = 5.00 msec) gave the original fall time of the test signal with an error of 0.8%. The next test was used to verify that the inverse of the waveform in Figure 29 should also work on the system.

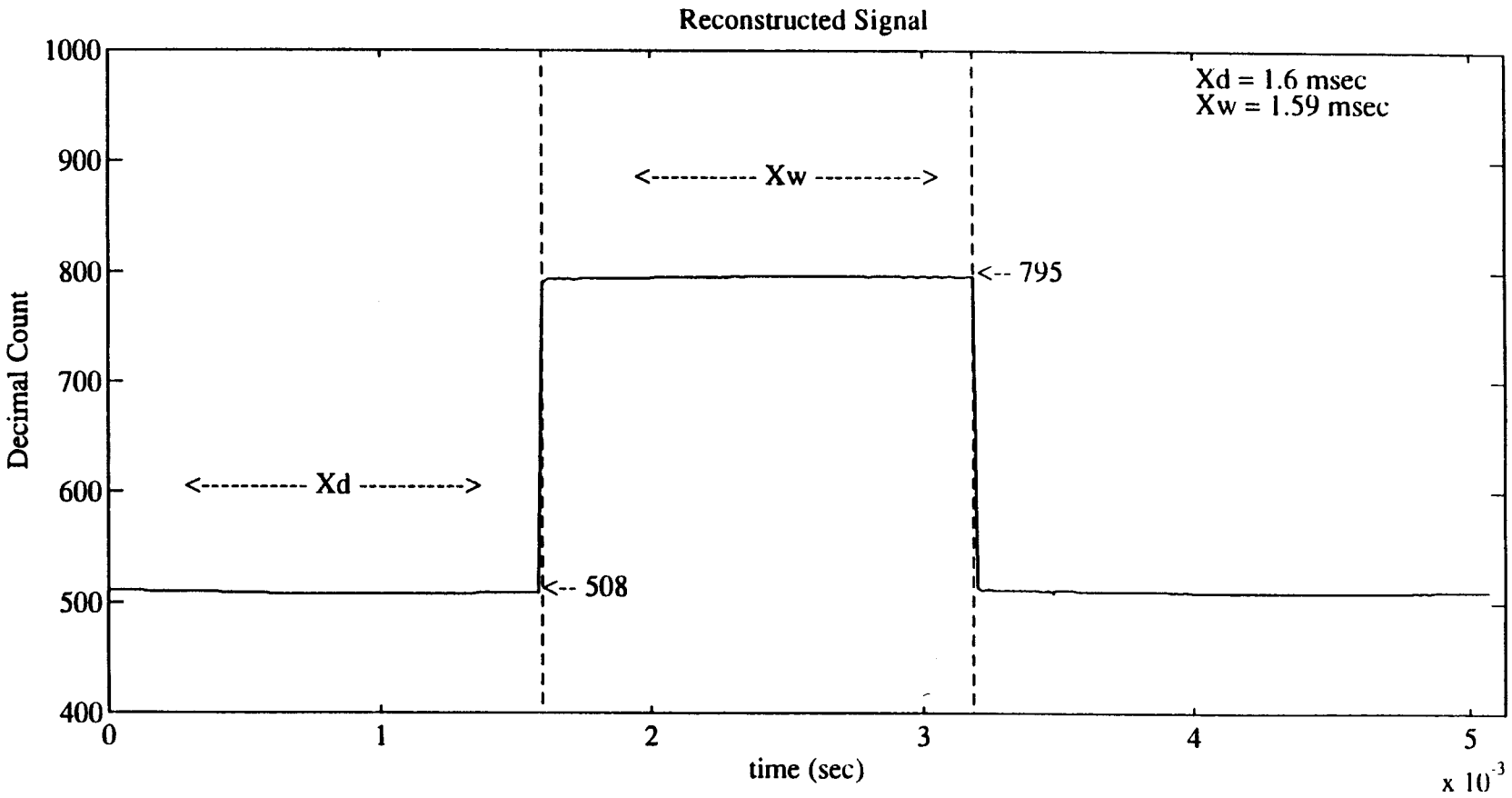
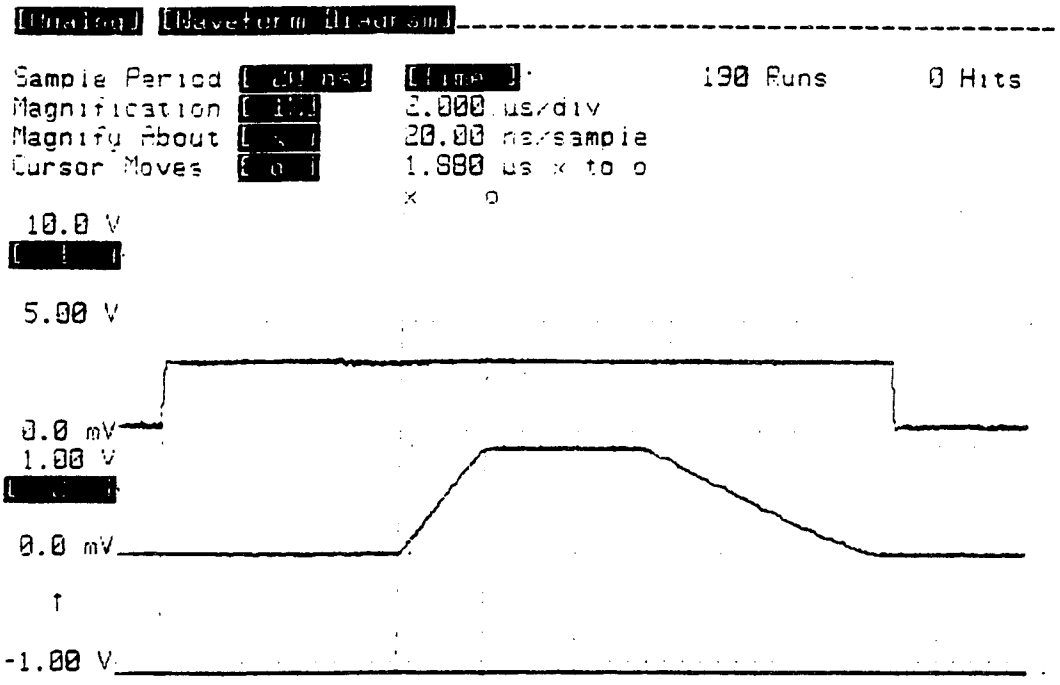
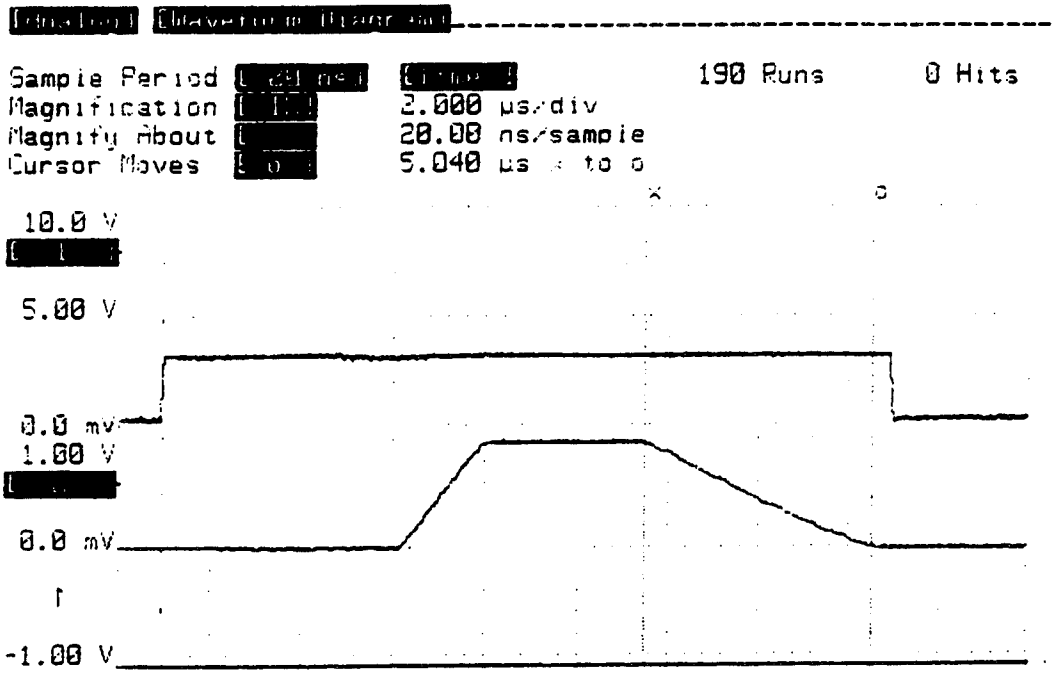


Figure 28. Reconstructed Signal for Complex Test Signal Waveform #1



(a)



(b)

Figure 29. Channel 1 Indicates the Burst Interval of 16.0 µsec, Whereas Channel 2 Indicates Test Signal Waveform

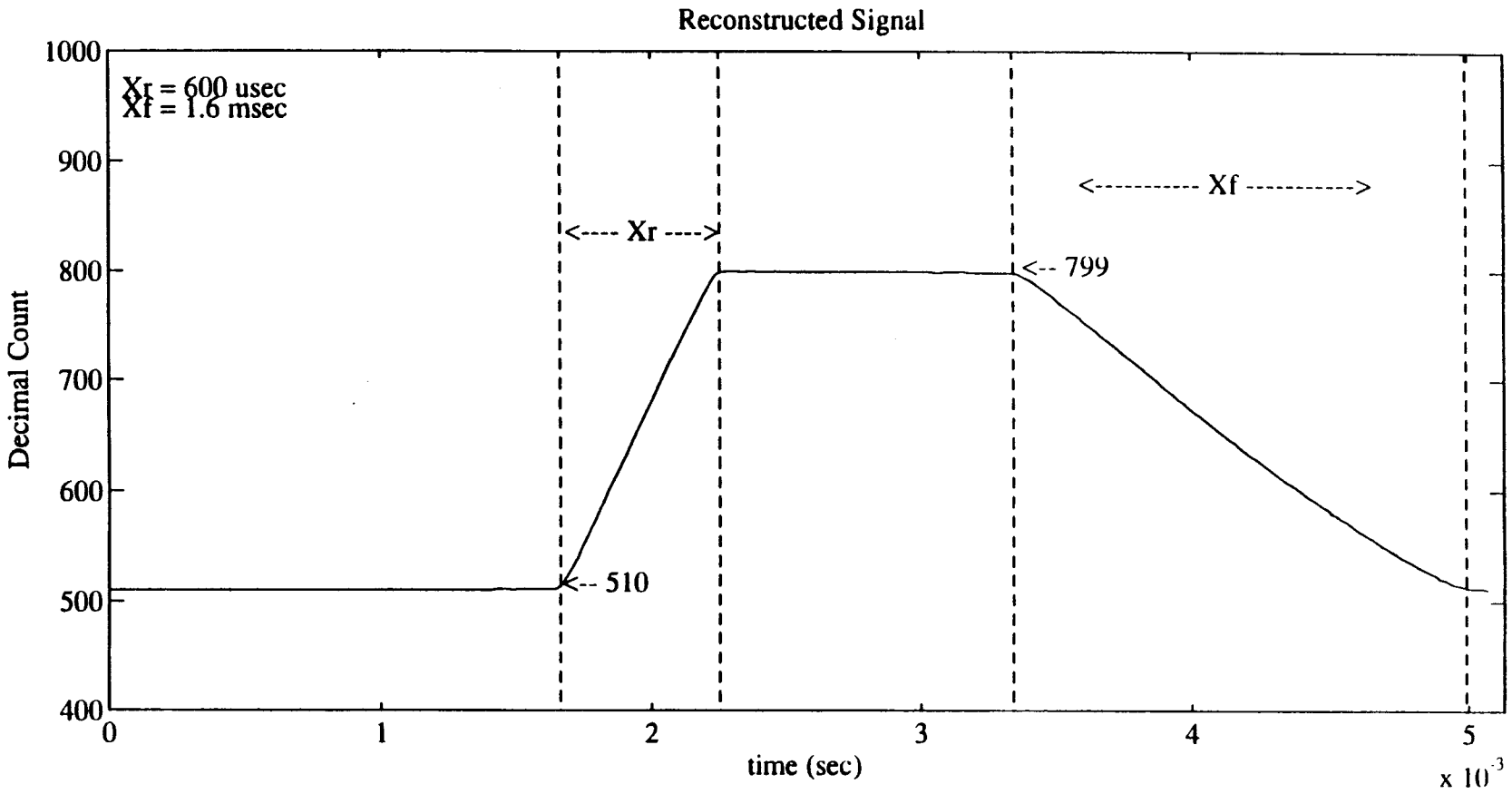
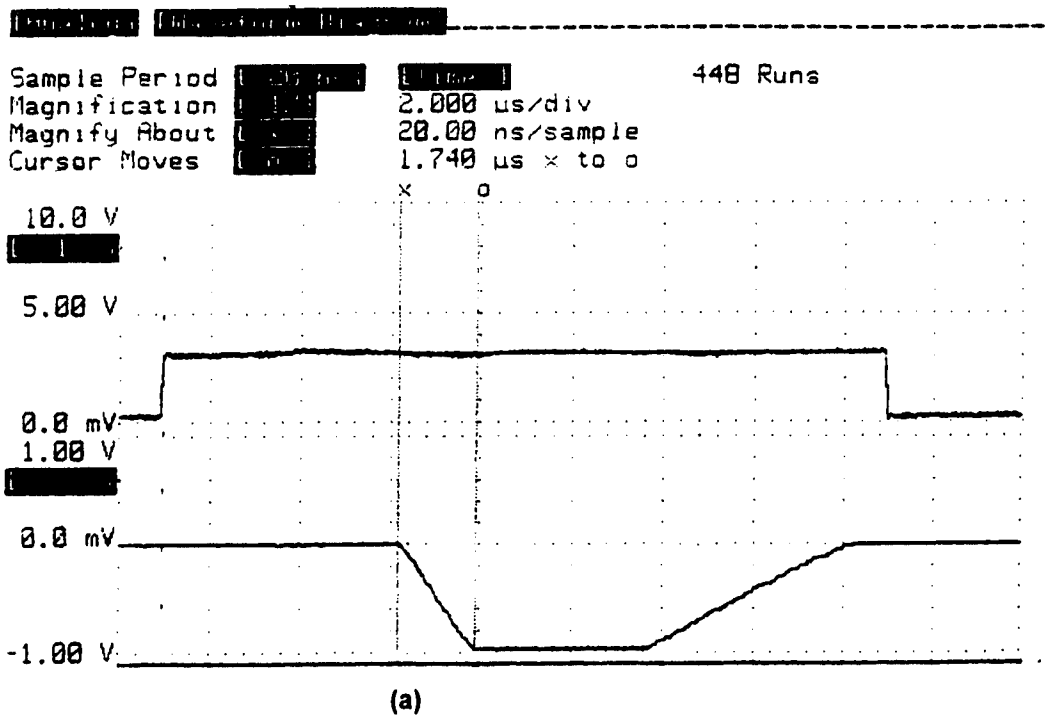


Figure 30. Reconstructed Signal for Complex Test Signal Waveform #2.

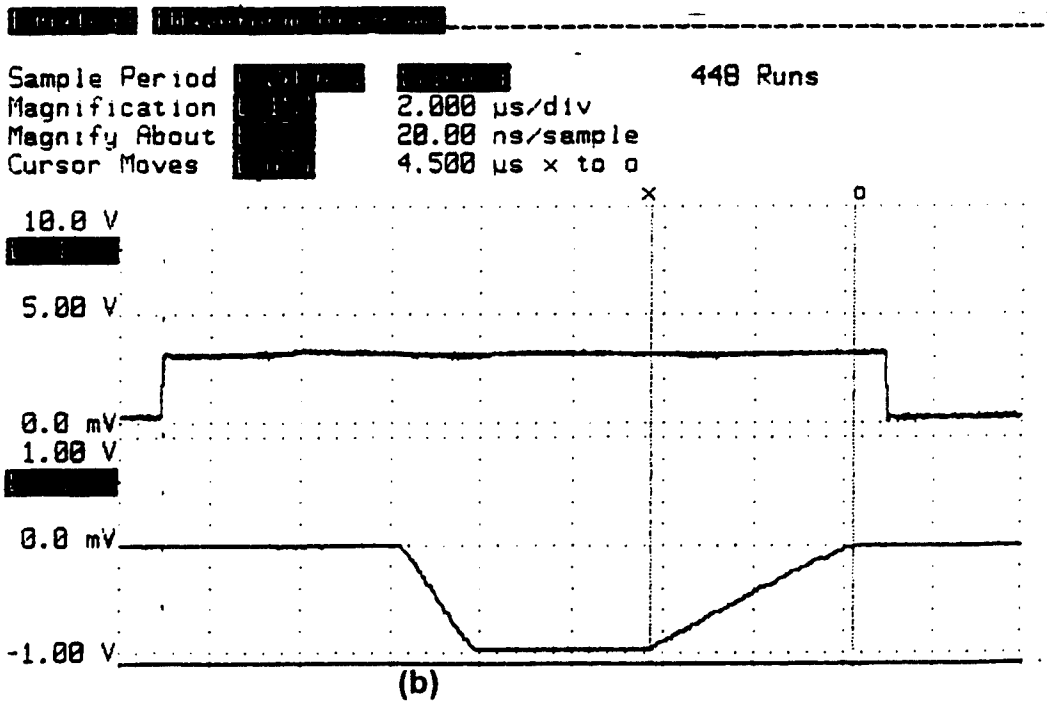
Figure 31 shows the test waveform of the inverse of Figure 29. Figure 31(a) shows the fall time of the tested signal, whereas Figure 31(b) shows the rise time of the tested signal. The fall and rise time were again measured for the reconstructed signal. In Figure 32, the reconstructed fall and rise time of the signal are displayed. The figure also shows the peak negative value of the waveform.

The next test signal used was an $e^{-t/t}$ waveform. The symbol t is the time constant of the waveform. To generate such a signal, a capacitor is placed in parallel with the output of the PHILIPS PM 5715 generator. Using the HP logic analyzer/digital oscilloscope, it was possible to capture the waveform. Figure 33 shows the waveform with a measured time of the increasing part of the pulse. To verify the measured time of the original signal, the reconstructed waveform was once again stored and displayed using the SYSTEM 9000. Figure 34 shows the value T which is the measured time of the increasing part of the reconstructed waveform. T divided by 320 gave a value of 6.9 μsec. The system has a percent error of 0.28% with $e^{-t/t}$ wave functions.

The final test used was the pseudo-random signal as shown in Figure 35; the figure shows a set of measurements of various portions of the signal. To verify the original waveform, a graph was plotted as shown in Figure 36. Here XI could be verified by dividing XI by 320 (XI/320 = 556 nsec) which corresponds approximately to the value in Figure 35(a) with a percent error of 0.7%. X2 could be divided by 320 to give a value of 600 nsec



(a)



(b)

Figure 31. Channel 1 Indicates the Burst Interval of 16.0 µsec, Whereas Channel 2 Indicates Test Signal Waveform

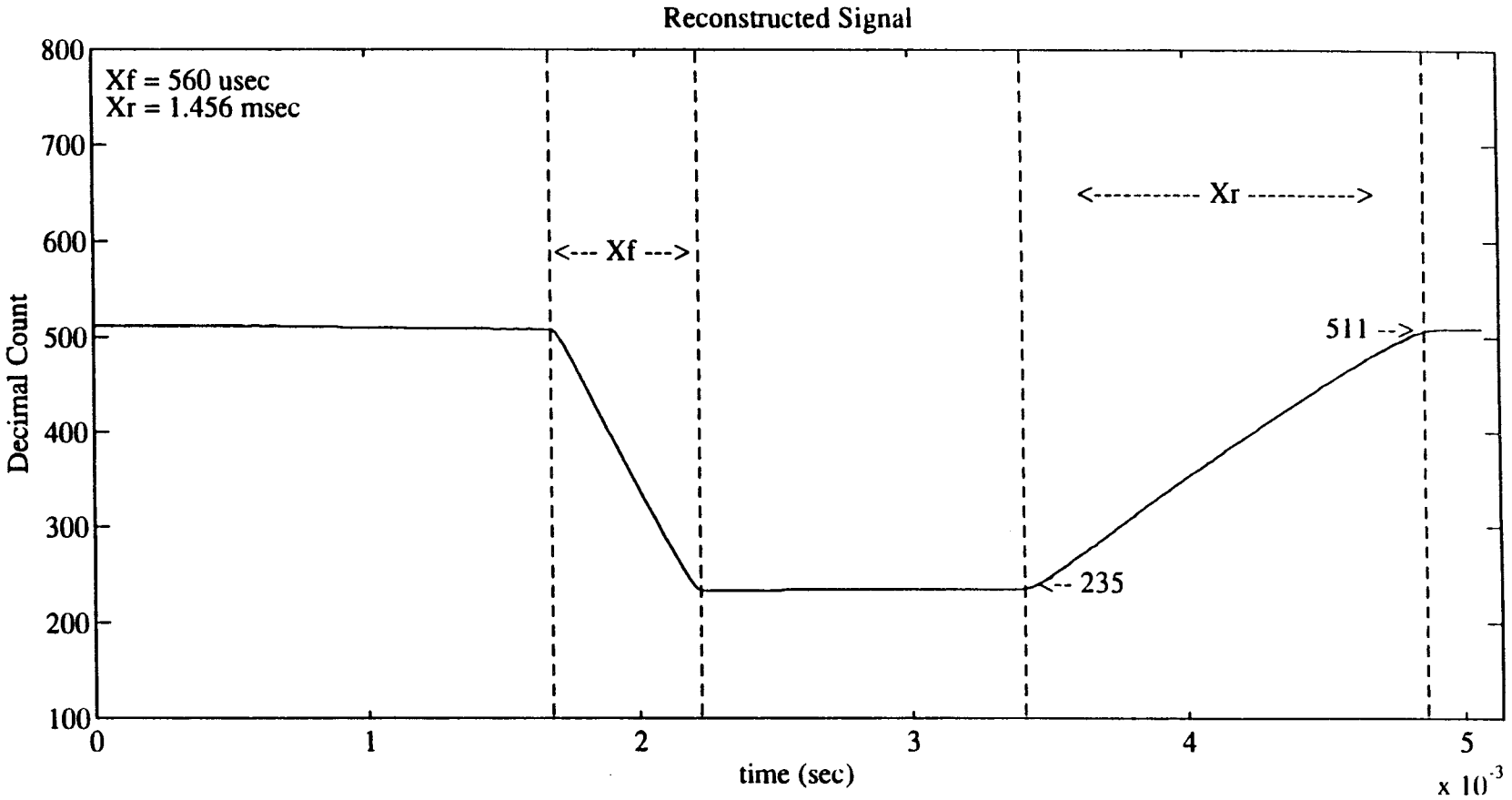


Figure 32 Reconstructed Signal for Complex Test Signal Waveform #3

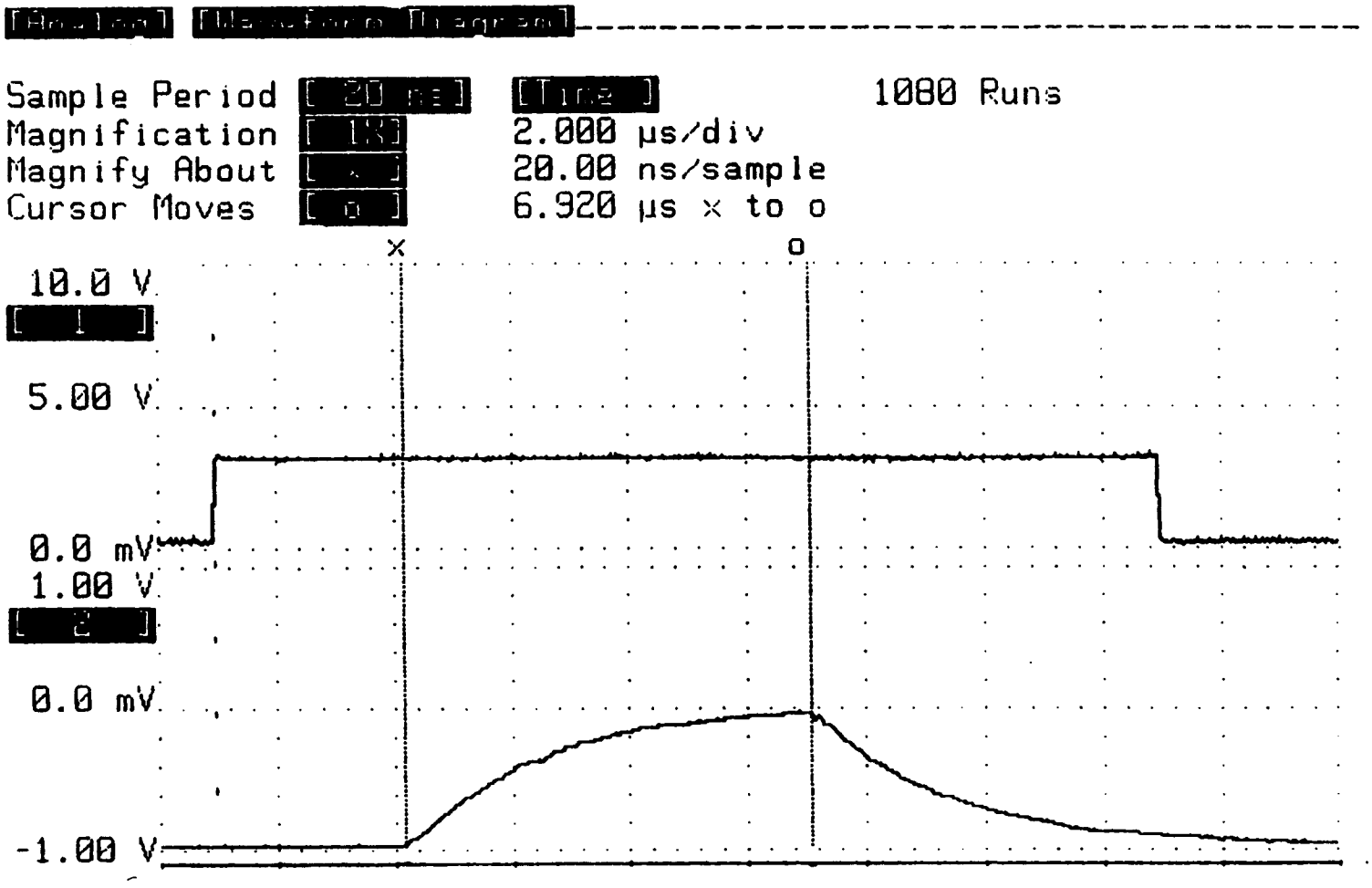


Figure 33. Channel 1 Indicates the Burst Interval of 16.0 µsec, Whereas Channel 2 Indicates Test Signal Waveform

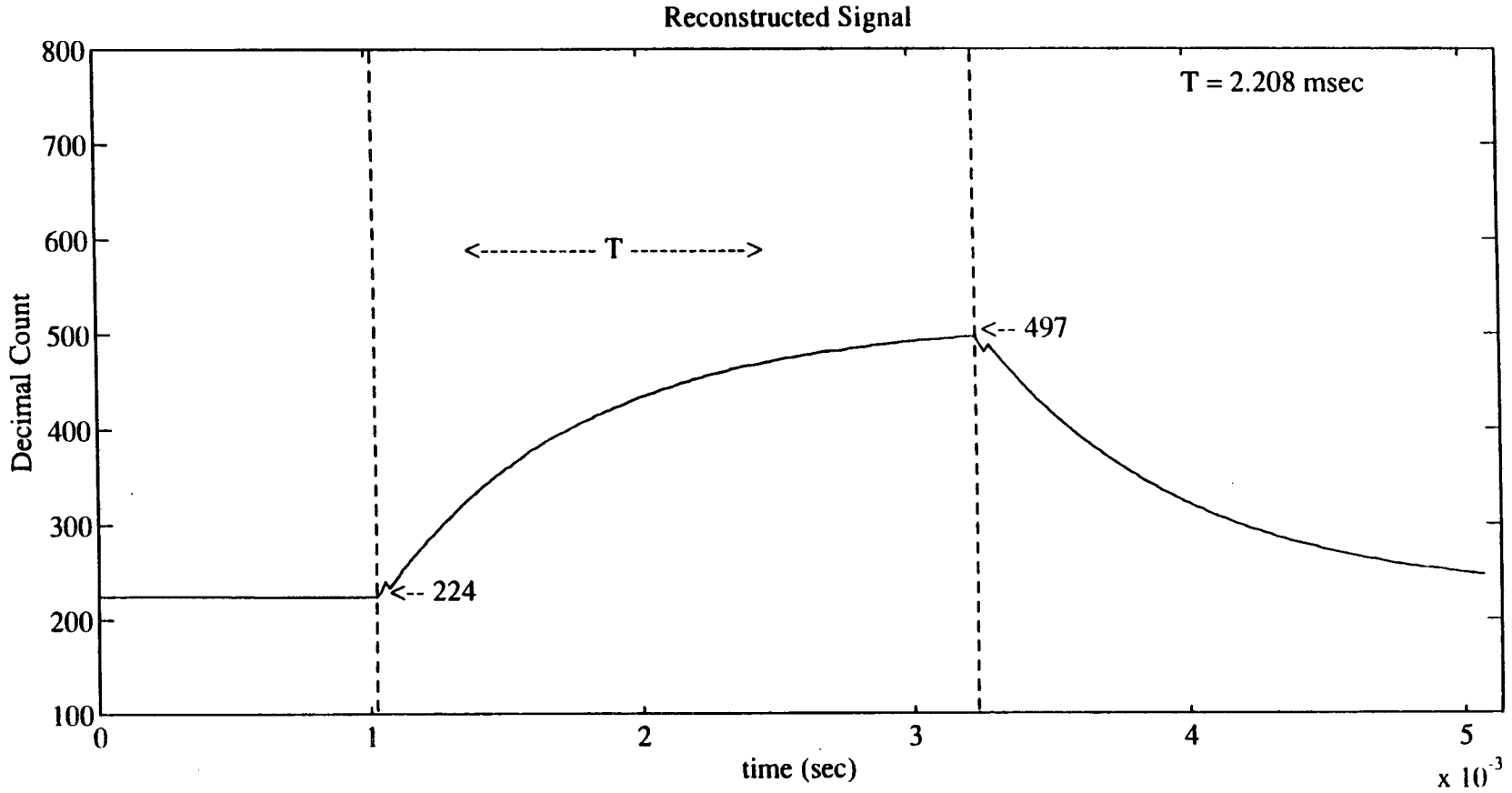


Figure 34. Reconstructed Signal for Complex Test Signal Waveform #4

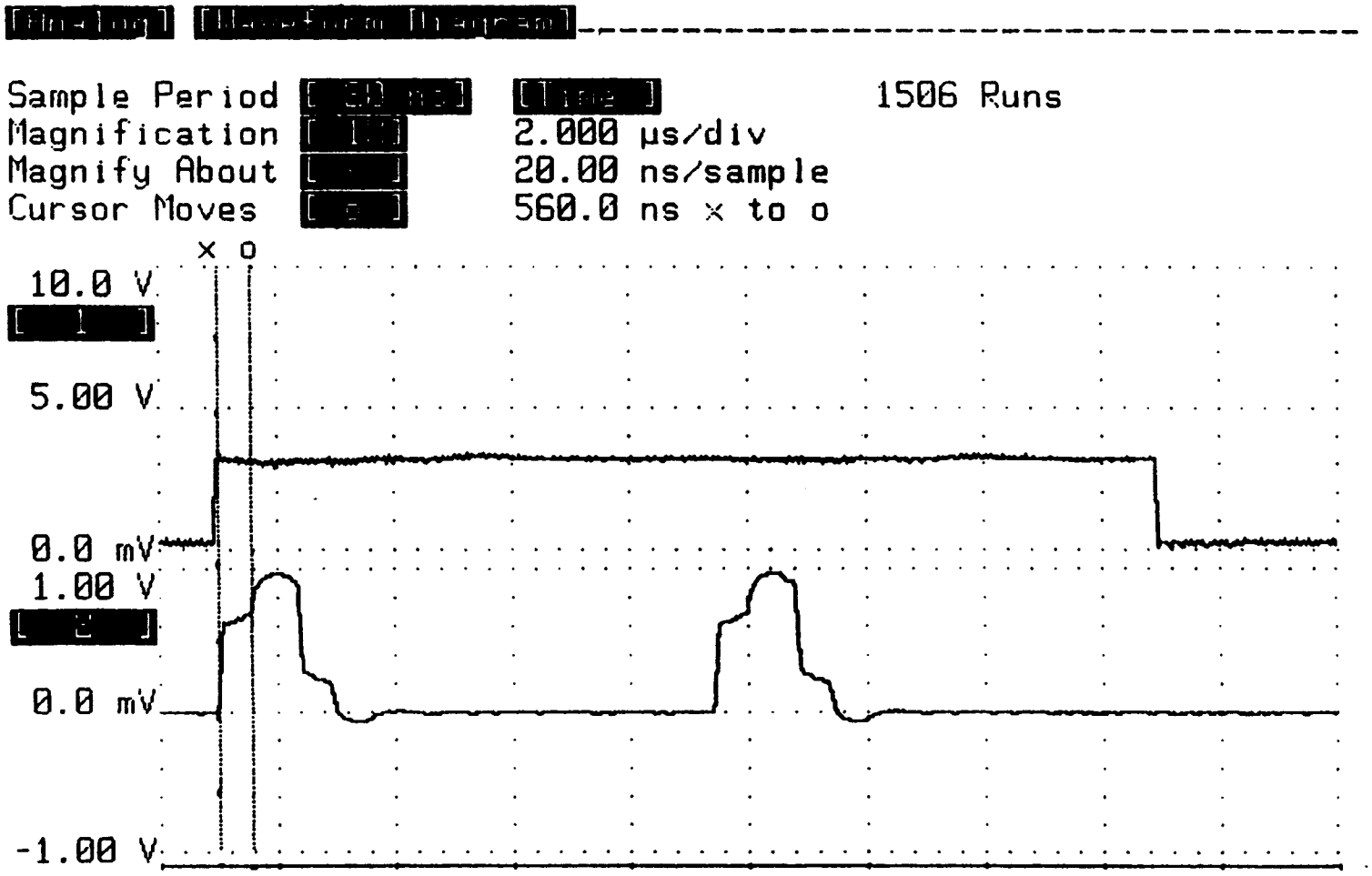


Figure 35(a). Channel 1 Indicates the Burst Interval of 16.0 µsec, Whereas Channel 2 Indicates Test Signal Waveform

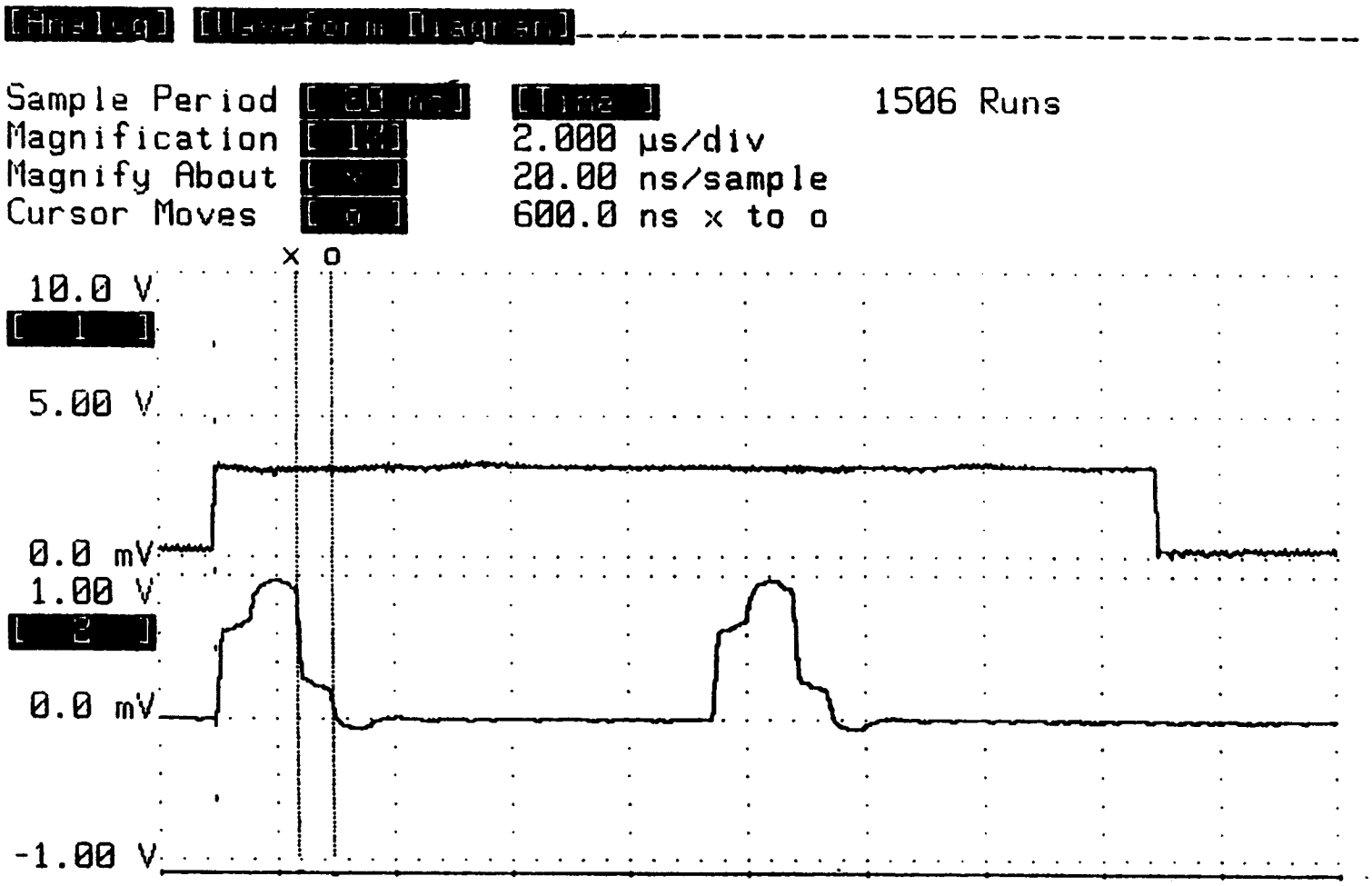


Figure 35(b). Channel 1 Indicates the Burst Interval of 16.0 µsec, Whereas Channel 2 Indicates Test Signal Waveform

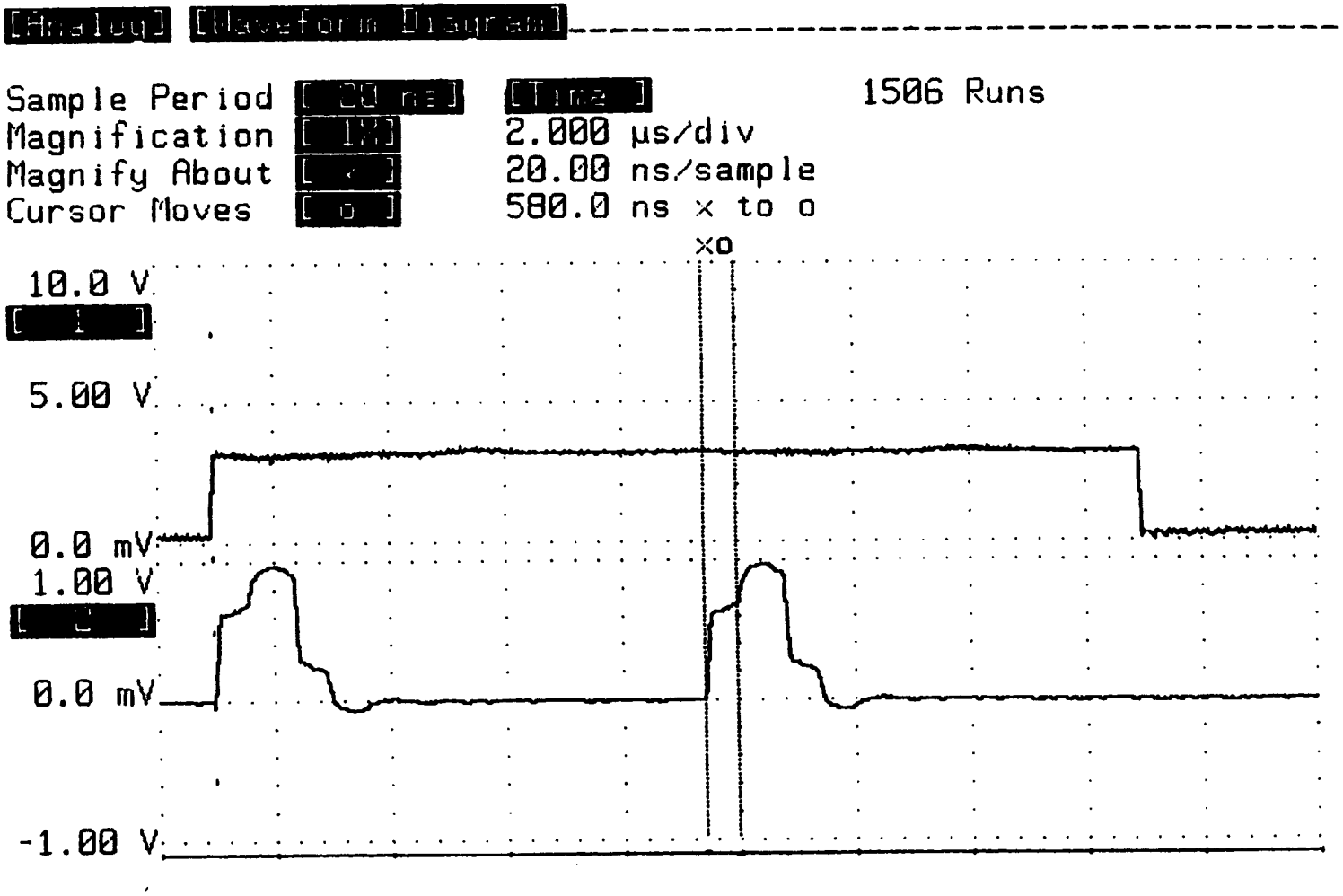


Figure 35 (c). Channel 1 Indicates the Burst Interval of 16.0 µsec, Whereas Channel 2 Indicates Test Signal Waveform

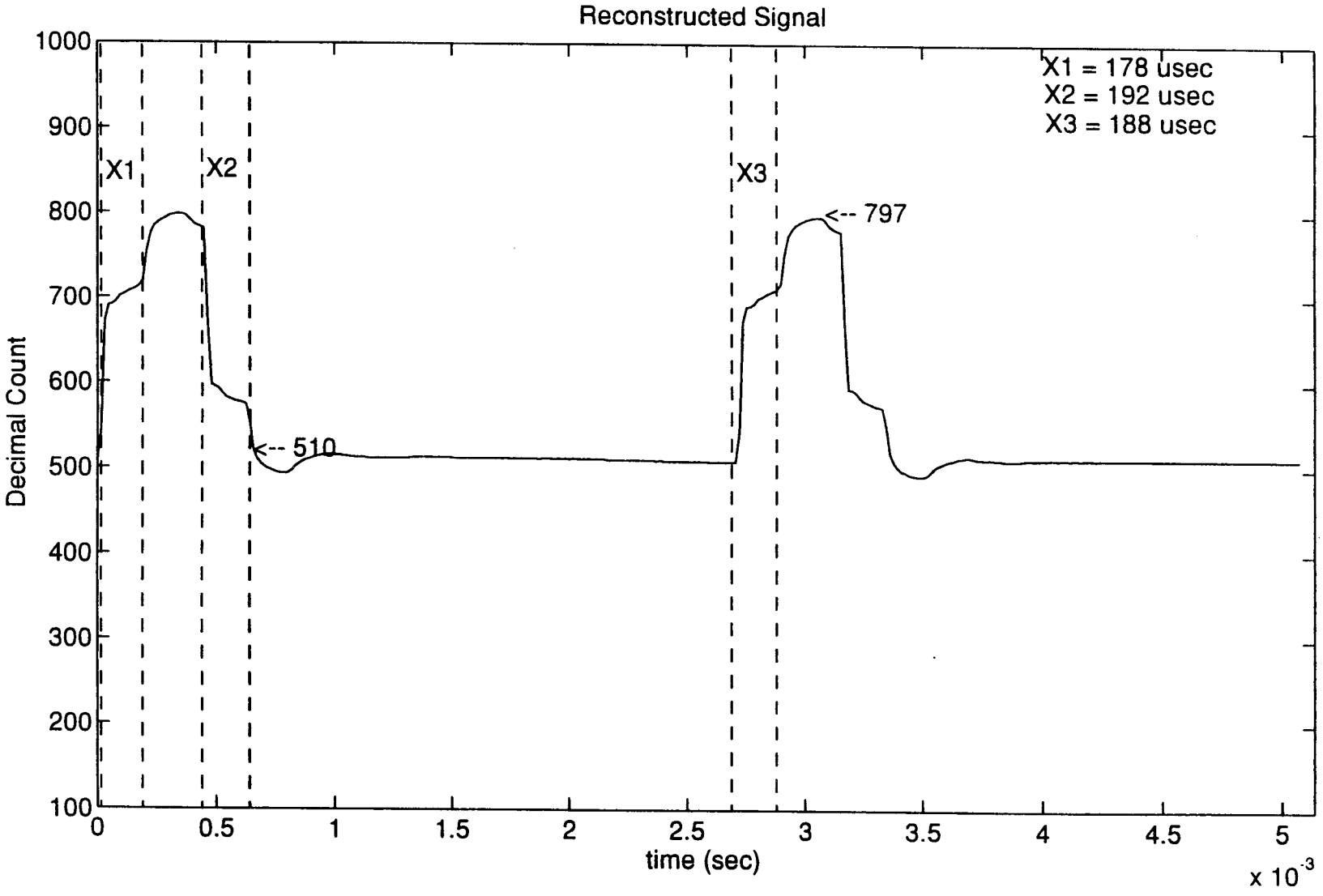


Figure 36. Reconstructed Signal for Complex Test Signal Waveform #5

which also verified the value of Figure 35(b). Finally, X3 is divided by 320 to give a value of 587 nsec which almost verified the value of Figure 35(c) with a percent error within 1.2%.

Overall, the integrated system works very well in situations with high-frequency content burst-type signals. These tests also demonstrated that burst-type phenomena with wait periods in between can be processed with an overall percent error not more than 1.2%. The accuracy of the measurements was probably limited by the capability of the test equipment used.

6. CONCLUSIONS AND RECOMMENDATIONS

In general, higher sampling rates require higher overall transmission bandwidth. It was demonstrated in this thesis that a lower rate PCM binary bit stream in r-f transmission is possible when burst-type data is encountered

During the burst interval of 16.0 μsec, the system sampled and stored the incoming signal. The stored data was converted into a serial bit stream during the wait period of 5.136 msec. Simultaneously, the serial bit stream was then stored into the SYSTEM 9000. The reconstructed signal from the SYSTEM 9000 was displayed and analyzed.

The results from the last chapter indicated that the data acquisition system in burst-type phenomena with wait periods in between are both reliable and accurate in a high-speed environment. Signals with fast rise and fall time, slow rise and fall time, $e^{t/\tau}$ wavefunction, and a pseudo-random signal can be used on such a system. The overall error of these reconstructed signals are

small, not more than 1.2%. The accuracy of the measurements was probably limited by the capability of the test equipment used.

To demonstrate the flexibility of the system, the system should be further tested with higher sampling rates. Since the AD9020/PCB is capable of sampling rates up to 60 MHz, a sampling rate higher than 20 MHz could be used on the system so that further analysis on the system can be made. The 10-bits resolution of the system can also be upgraded when higher bit commercial converters with capability of high conversion speed and dynamic performance are made both available and more affordable. The test measurements made on the system can also be improved by using more advance test equipment. Finally, the system could also be tested with more complicated signals, such as video signals, so that the behavior of the system can be further evaluated.

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RELATED CONTRACTS AND PUBLICATIONS

F19628-87-C-0128 1 July 1987 - 31 March 1991

F19628-91-C-0012 20 January 1991 - Present

J. S. Rochefort, L. J. O'Connor, R. Sukys, N. C. Poirier, R. L. Morin, (1991), *Instrumentation, Control, and Communication Systems for Sounding Rockets and Shuttle-Borne Experiments*, Final Report, F19628-87-C-0128, PL-TR-91-2175, ADA241272.

PERSONNEL

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